REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

DEVICE ORDER INFORMATION

SCT2460FRA	2460	QFN-10L

1) For Tape & Reel, Add Suffix R (e.g. SCT2460FRAR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted[1]

RT/CLK	6	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
SS	7	Connect a cap to ground, program the soft start time.
EN	8	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN	9	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
SW	10	Regulator switching output. Connect SW to an external power inductor

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range			

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		3.8		36	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		3.5 400	3.7	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1	5	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		25		μA
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		36		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			13		mΩ
V_{REF}	Reference voltage of FB		0.792	0.8	0.808	V
G_{EA}	Error amplifier trans-conductance	-2μA<I_{COMP}<2μA, V_{COMP}=1V		300		μS
I_{COMP_SRC}	EA maximum source current	V_{FB}=V_{REF}-100mV, V_{COMP}=1V		30		μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=V_{REF}+100mV, V_{COMP}=1V		30		μA
V_{COMP_H}	COMP high clamp			3		V
V_{COMP_L}	COMP low clamp			0.4		V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		8	9	10	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold			9		A
T_{HIC_W}	Over current protection hiccup wait time			512		cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		cycles
V_{EN_H}	Enable high threshold			1.18	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
V_{EN_HYS}	Enable threshold hysteresis			80		mV
I_{EN_L}	Enable pin pull-up current	EN=1V	1	1.5	2	μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		uA
Iss	SS pin current			3		uA
F_{RANGE_RT}	Frequency range using RT mode *		100		2200	KHz
F_{SW}	Switching frequency	R_{RT}=200 kΩ(1%)	450	500	550	KHz
F_{RANGE_CLK}	Frequency range using CLK mode *		100		2200	KHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%

t

TYPICAL CHARACTERISTICS

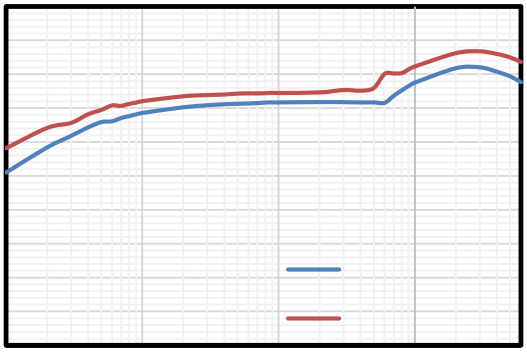


Figure 2. Efficiency vs Load Current, Vin=36V

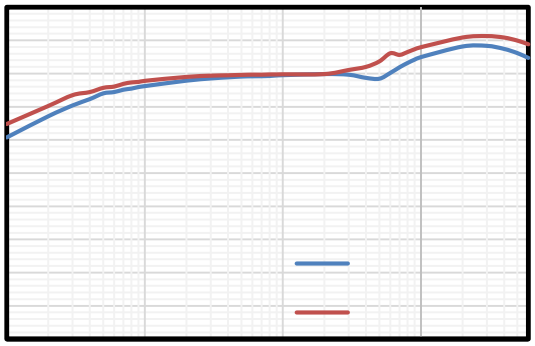


Figure 3. Efficiency vs Load Current, Vin=24V

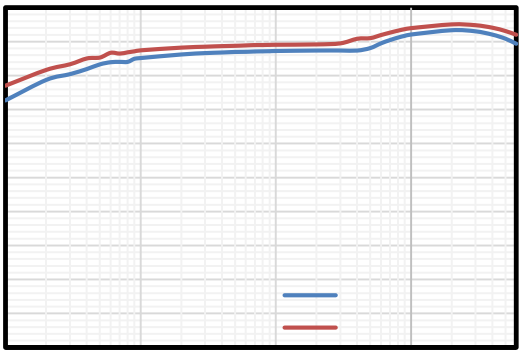


Figure 4. Efficiency vs Load Current, Vin=12V

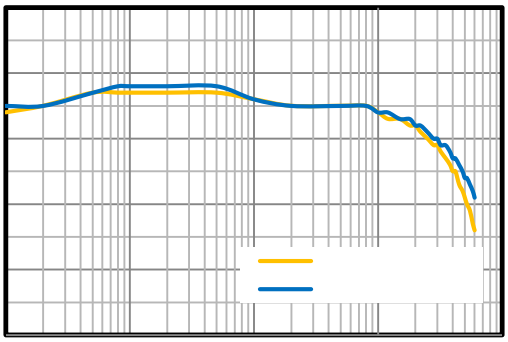


Figure 5. Load Regulation (Vout=5V)

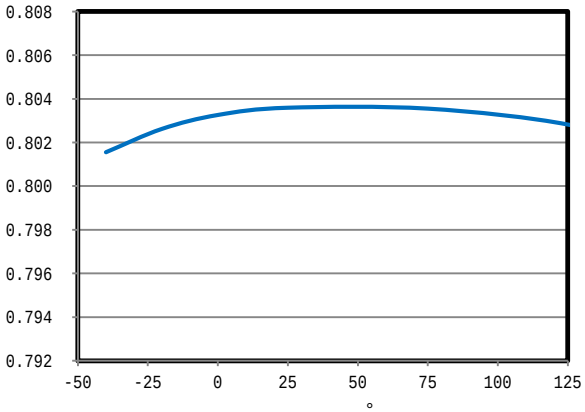


Figure 6. Reference Voltage vs Temperature

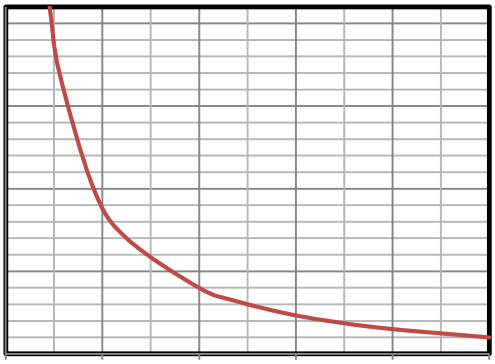


Figure 7.Clock Frequency vs RT/CLK Resistor

FUNCTIONAL BLOCK DIAGRAM

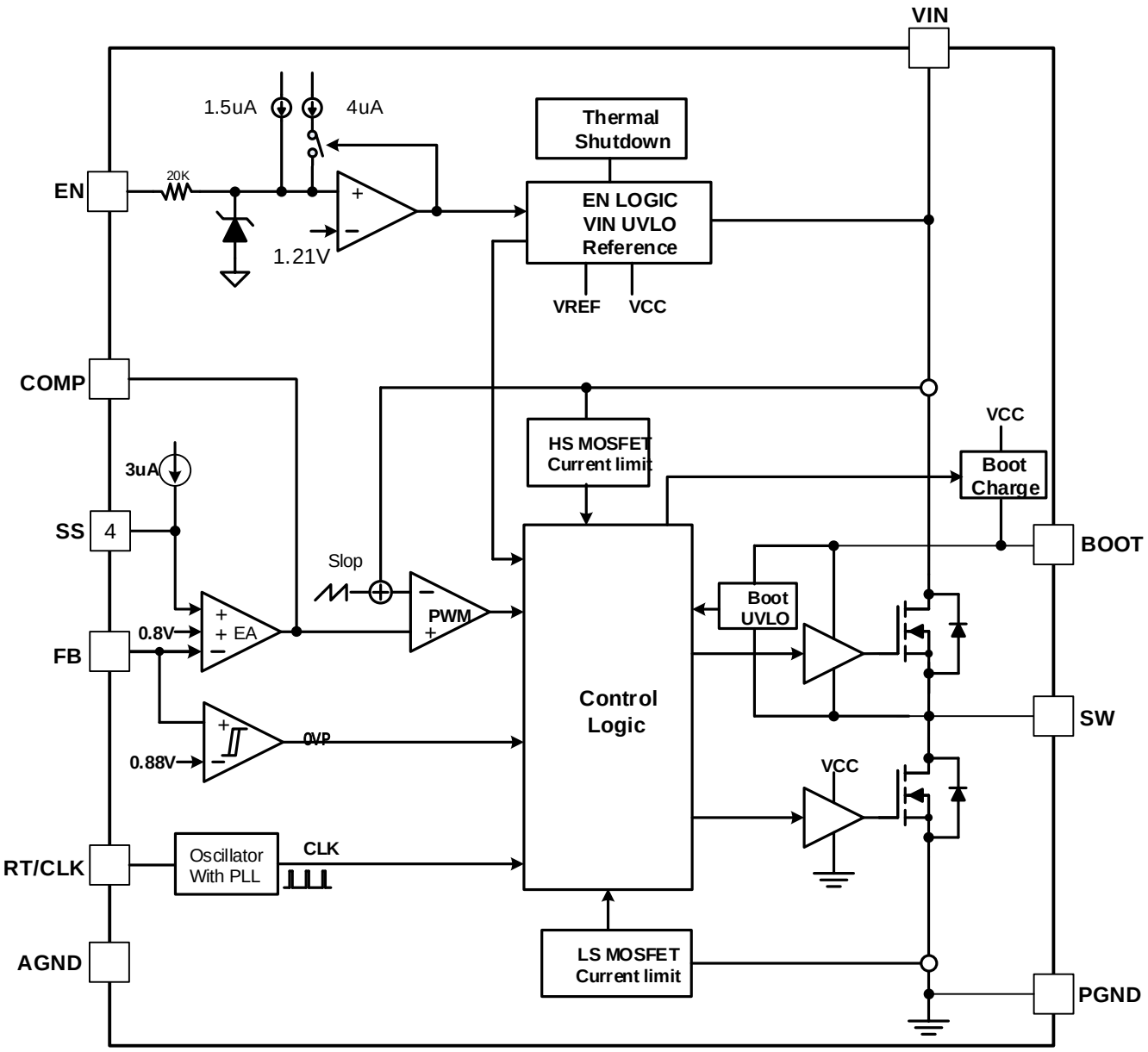


Figure 8. Functional Block Diagram

below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = \frac{R1 + R2}{R2} \times 1.21V \qquad (1)$$

$$V_{fall} = \frac{R1 + R2}{R2} \times 1.21V - R1 \times 20K \qquad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

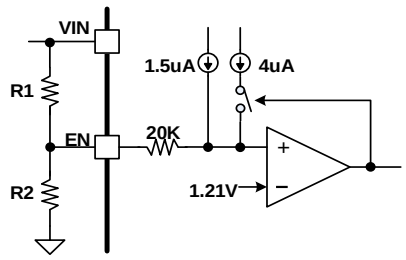


Figure 9. System UVLO by enable divide

The SCT2460 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_{FB\_TOP}}{R_{FB\_BOT}}\right) \qquad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

The SCT2460 features programmable soft-start time to prevent inrush current during start-up stage. The soft-start time can be programmed easily by connecting a soft-start capacitor C_{ss} (C_{ss} is the C13 on Figure 9) from SS pin to ground.

The SS pin sources an internal 3µA current charging the external soft-start capacitor C_{ss} when the EN pin exceeds turn-on threshold. The device adopts the lower voltage between the internal voltage reference 0.8V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 0.8V.

The soft-start capacitor value can be calculated going with following equation 4. Attention should be taken here that the programmed soft-start time should be larger than 4ms.

$$C_{SS} = \frac{t_{ss} \times 3\mu A}{0.8V} \qquad (4)$$

Where:

- C_{SS} is the soft-start capacitor connected from SS pin to the ground
- t_{ss} is the soft-start time

The switching frequency of the SCT2460 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 2.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 5 or the plot in Figure 10 to determine the resistance for a switching frequency

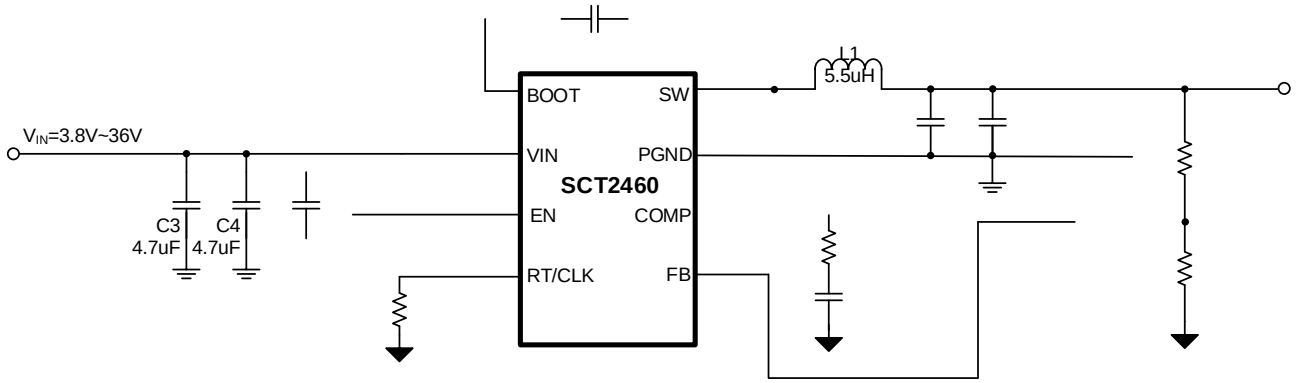
Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2460 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Figure 11. LDO Operation Characteristic (Vout =5V)

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2460 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 3.7V typical. When COMP voltage is clamped for 512 cycles, the converter stops switching. After remaining OFF for 8192 cycles the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high for 512 cycles the device enters into turning-off mode again. When overload or hard short condition is removed, the device as

APPLICATION INFORMATION



Input Voltage	24V Normal 3.8V to 36V
Output Voltage	3.3V
Maximum Output Current	6A
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	20mV
Transient Response 1.5A to 4.5A load step	ΔVout = 200mV
Start Input Voltage (rising VIN)	5.76V
Stop Input Voltage (falling VIN)	4.66V

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 6 to calculate R5.

$$4_9 \; L \; I \frac{8_E \; \hat{I} \; \acute{I}}{8_E \; ¾ \; ¿} \; F \; sp \; \hat{U} 4 \qquad (6)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

1.8 V	12.7 KΩ	10.2 KΩ
2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrads converter's overall power efficiency and thermal performance. The 100ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design a moderate switching frequency of 500 KHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 6, or determined from Figure 7.

$$4_7 : \; 3 ; \; L \; \frac{s \; r \; r \; r \; r \; r}{\hat{} \bullet ™ \; : \; œ \; ;} \qquad (7)$$

where:

- f_{SW} is the desired switching frequency

200 KHz	500 KΩ
330 KHz	301 KΩ
500 KHz	200 KΩ
1100 KHz	90.9 KΩ

higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 10.

$$\Delta I_{LPP} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot f_{SW} \cdot V_{IN}} \quad (10)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 11 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} \cdot \Delta I_{LPP}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (11)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 12 and equation 13.

$$I_{LPEAK} = I_{OUT} + \frac{\Delta I_{LPP}}{2} \quad (12)$$

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \cdot \Delta I_{LPP}^2} \quad (13)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 8A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2460 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.2 or 0.3, and the inductor value is calculated to be 5uH, the RMS inductor current is 6A and the peak inductor current is 7.2A. The chosen inductor is a WE 744325550, which has a saturation current

$$\hat{É}7 \; L \; \frac{s}{t\,è\,Û\%\;Û4_8} \tag{24}$$

The crossover frequency of converter is shown in Equation 25.

$$\hat{¼} \; L \; \frac{8_{¿\,»}}{8_{È\,Î\,Í}} \; Û \frac{)\,¾\,º\,Ü)_{Â\,Ì\,Ç\,Ì}\,Ü4_8}{t\,è\,Û\%_{È\,Î\,Í}} \tag{25}$$

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R4 with Equation 26 once crossover frequency is selected.

$$4_8 \; L \; \frac{8_{È\,Î\,Í}}{8_{¿\,»}} \; Û \frac{t\,è\,Û\%_{È\,Î\,Í}\;ÛB_{¾}}{)\,¾\,º\,Û)_{Â\,Ì\,Ç\,Ì}} \tag{26}$$

Then calculate C7 by placing a compensation zero at or before the output stage pole.

$$\%_{¸} \; L \; \frac{4_{Â\,È\,º\,½}\,Û\%_{È\,Î\,Í}}{4v} \tag{27}$$

Determine if the optional compensation capacitor C6 is required. Generally, it is required if the ESR zero f_{Z2} is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C6 can be calculated with Equation 28.

$$\%_{¸} \; L \; \frac{\%_{È\,Î\,Í}\;H\,'\,5\,4}{4_8} \tag{28}$$

Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions not list in Table 3, customers can use Equation 25-Equation 27 to optimize the compensation components.

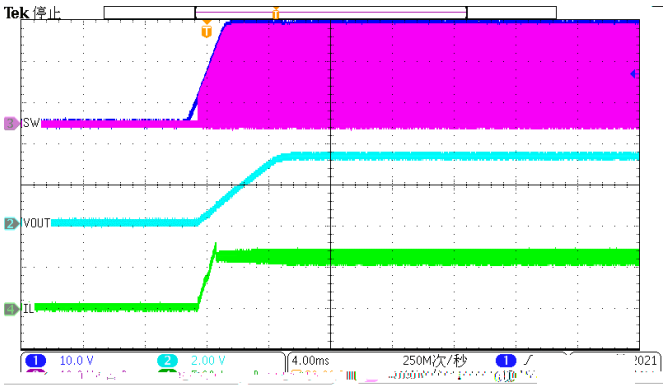


Figure 13. Power up (Iload=6A)

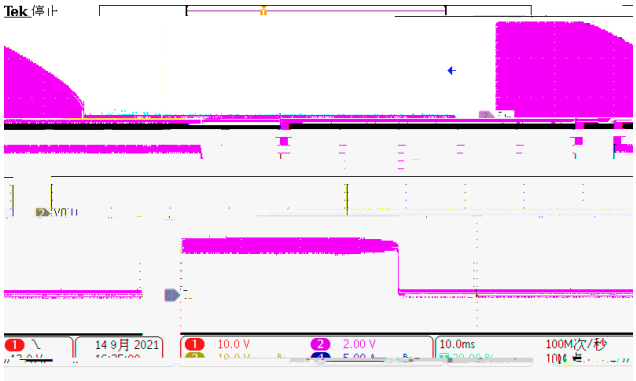


Figure 14. Power down (Iload=6A)

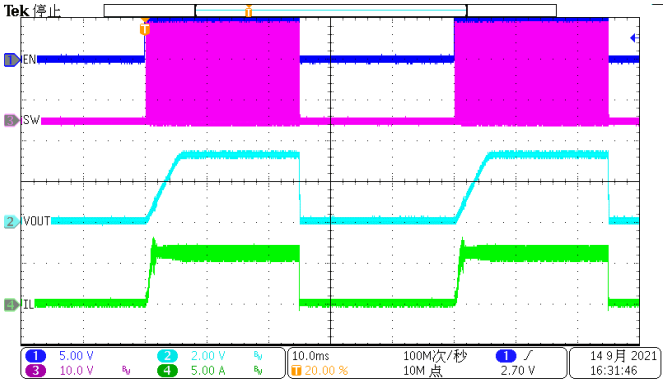


Figure 15. EN toggle (Iload=6A)

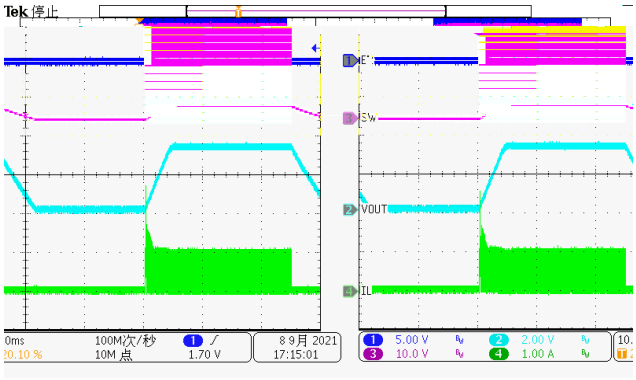


Figure 16. EN toggle (Iload=100mA)

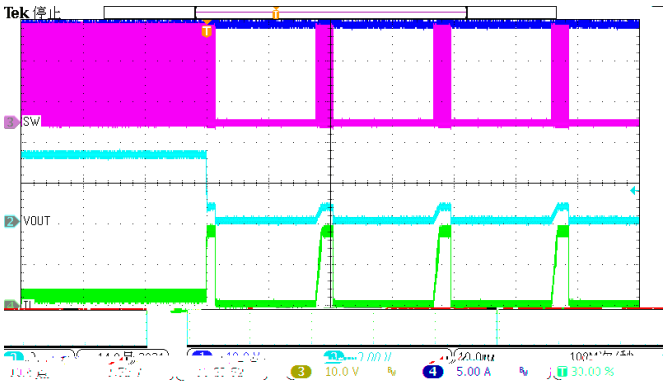


Figure 17. Over Current Protection(1A to hard short)

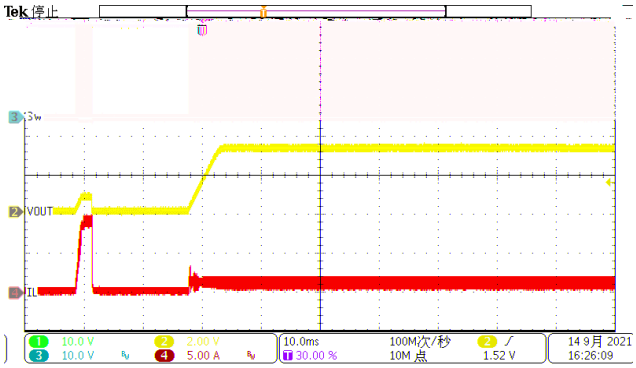


Figure 18. Over Current Release (hard short to 1A)

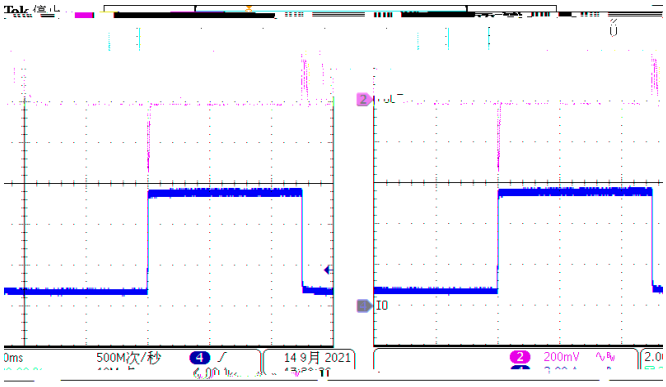


Figure 19. Load Transient (0.6A-5.4A, 1.6A/us)

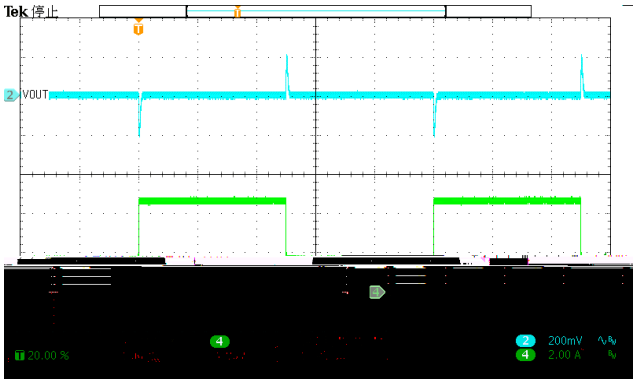


Figure 20. Load Transient (1.5A-4.5A, 1.6A/us)

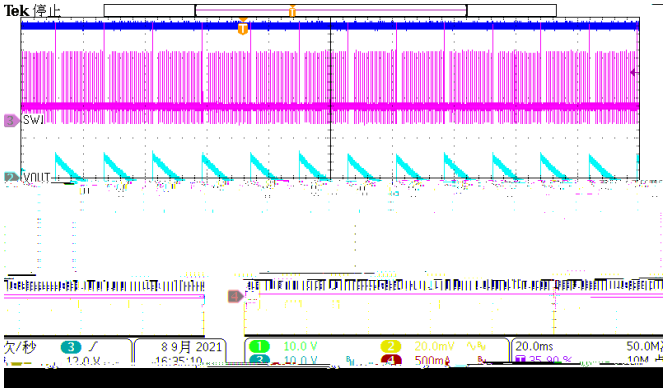


Figure 21. Output Ripple (Iload=0A)

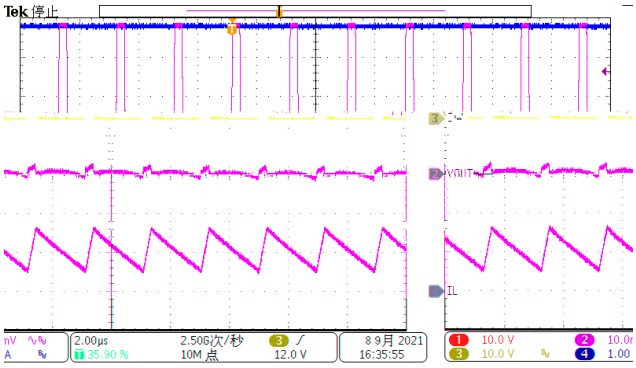


Figure 22. Output Ripple (Iload=100mA)

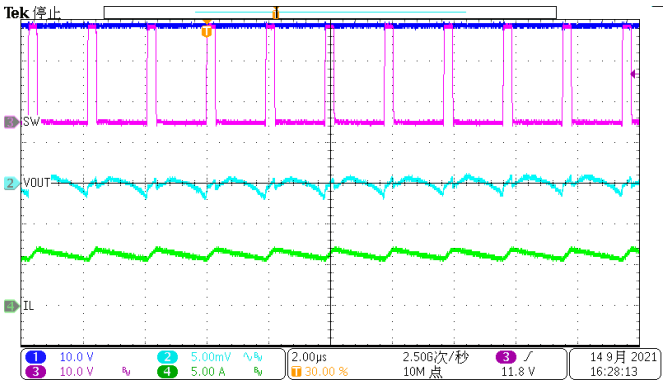


Figure 23. Output Ripple (Iload=6A)

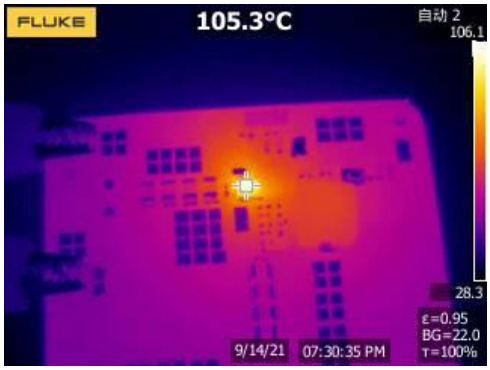


Figure 24. Thermal, 12VIN, 3.3Vout, 6A

Proper PCB layout is a critical for SCT2460's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

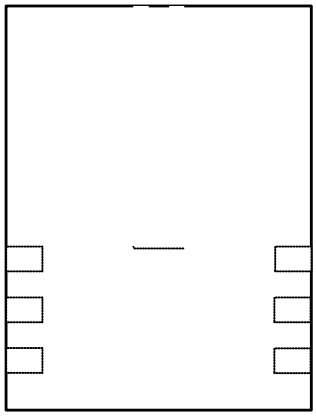
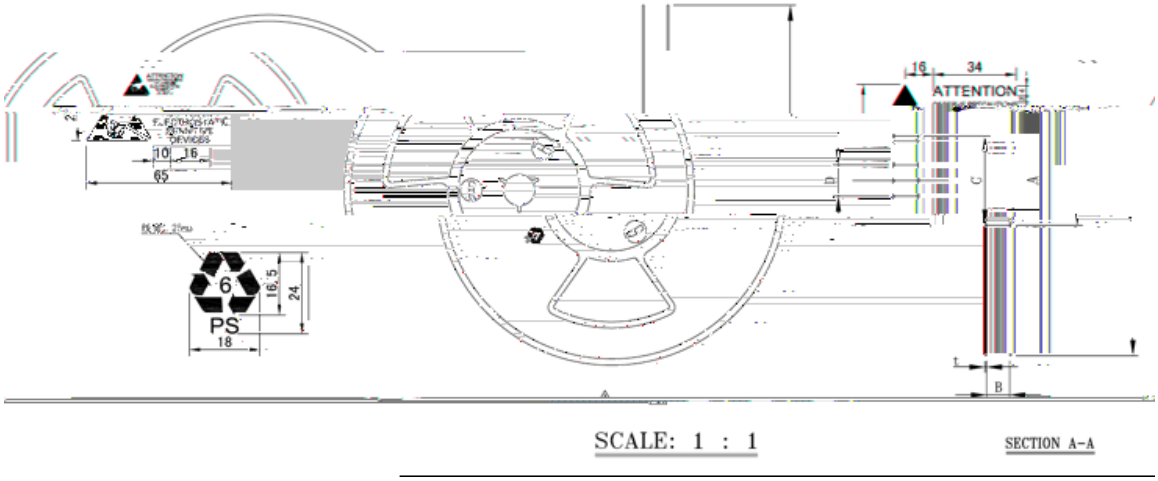


Figure 25. PCB Layout Example

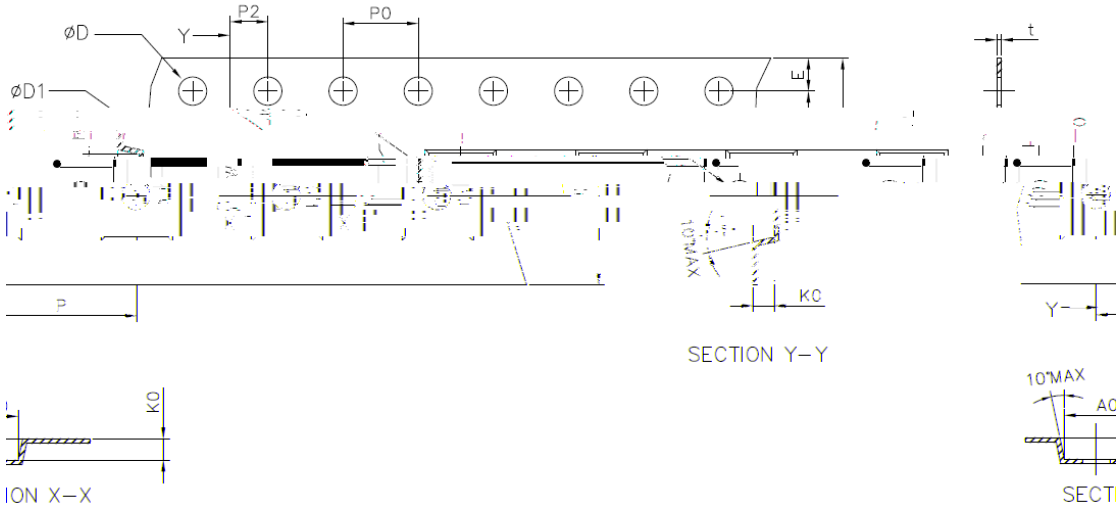
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT2460FRAR	QFN 3mmx4mm	10	5000



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TAPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12	3.40±0.10	4.40±0.10	1.14±0.10	0.25±0.02	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.05	2.00±0.05	1.50	1.50	4.00±0.10	40.0±0.20

