NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

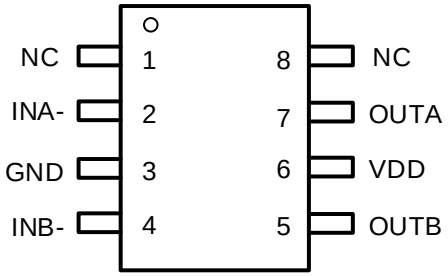
PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT52243STDR	2243	SOP-8

1 For Tape & Reel, Add Suffix R (e.g. SCT52243STDR).

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
INA-, INB-	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
VDD	-0.3	26	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

Top View: SOP-8pin
Plastic



(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

NAME	NO.	PIN FUNCTION
NC	1	No Connection.
INA-	2	Channel A logic input, TTL compatible. Floating logic low.
GND	3	Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact.
INB-	4	Channel B logic input, TTL compatible. Floating logic low.
OUTB	5	Channel B gate driver output
VDD	6	Power Supply, must be locally bypassed by the ceramic cap.
OUTA	7	Channel A gate driver output
NC	8	No Connection.

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA-,INB-}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	SOP-8L	UNIT
R	Junction to ambient thermal resistance (1)	130	°C/W
R	Junction to case thermal resistance (1)	80	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT52243 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT52243. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Supply current	V_{DD}=12V, INA- =INB- =GND V_{DD}=12V, INA-		130		uA

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

V_{IN}=12V, T_A= 25°C.

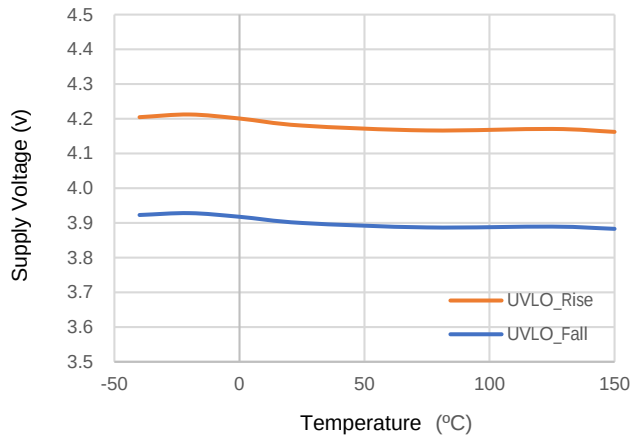


Figure 1. UVLO vs Temperature

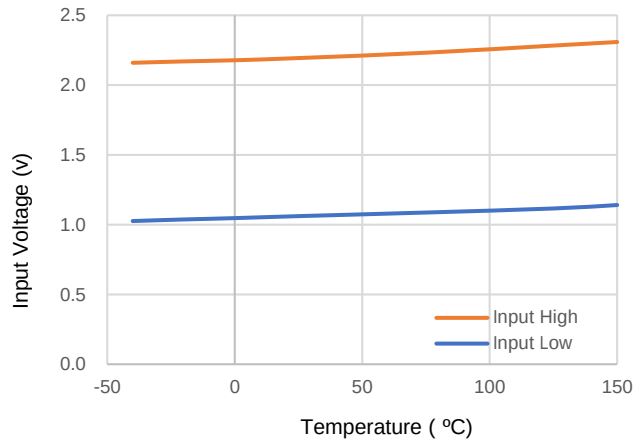


Figure 2. Input Threshold vs Temperature

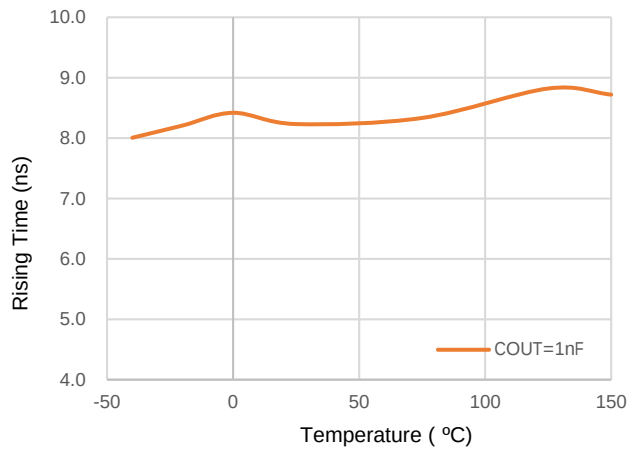


Figure 3. Output Rising Time vs Temperature

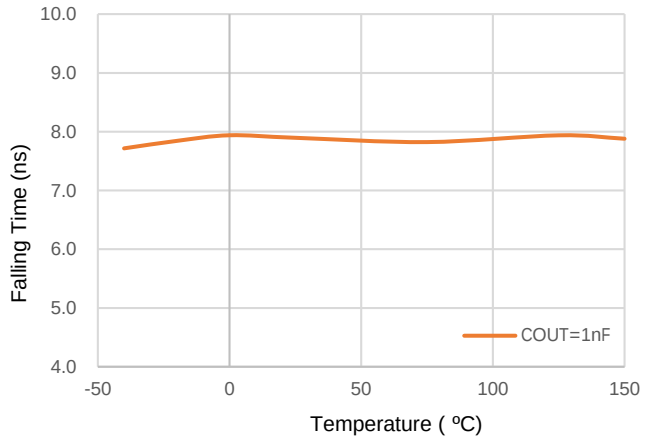


Figure 4. Output Falling Time vs Temperature

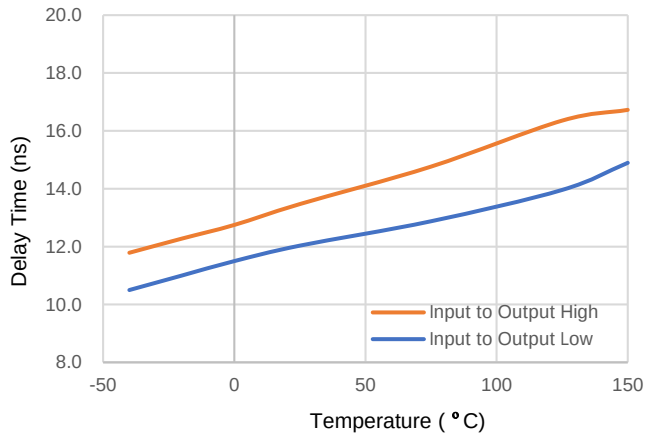


Figure 5. Input to Output Propagation Delay vs Temperature

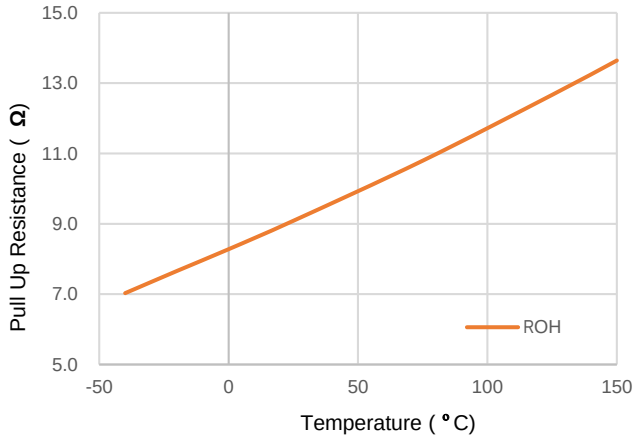


Figure 6. ROH vs Temperature

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

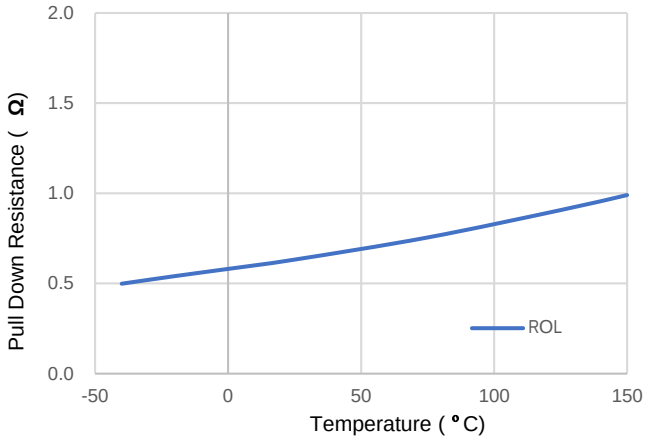


Figure 7. ROL vs Temperature

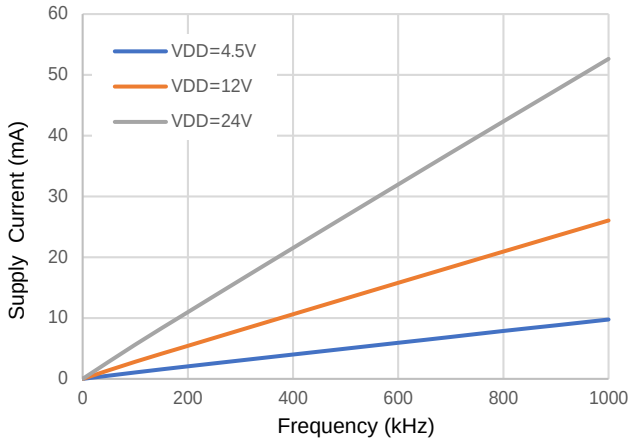


Figure 8. Operation Supply Current vs Frequency, C_{OUT}=1nF

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Overview

The SCT52243 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52243 output stage robustness during switching load fast transition. Table 1 shows the device output logic truth table.

Table 1: the SCT52243 Device Logic.

INA-	INB-	OUTA	OUTB
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	L
Any(UVLO)	Any(UVLO)	H	H
Floating	Floating	H	H
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	L

VDD Power Supply

The SCT52243 operates under a supply voltage range between 4.5V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1- F surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT52243. In addition, a larger capacitor (such as 1- F or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Under Voltage Lockout (UVLO)

SCT52243 device Under Voltage Lock Out (UVLO) rising threshold is typically 4.2 V with 300-mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output high regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise from the power supply.

Input Stage

The input of SCT52243 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

than 0.5V. SCT52243 also features tight control of the input pin threshold voltage that ensures stable operation across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

Output Stage

The SCT52243 output stage features the pull up structure with P-type MOSFET PM1 and N-type MOSFET NM1 in parallel, as shown in Figure 12. PM1 provides the pull up capability when OUT approaches VDD and the NM1 holds off state, which guarantees the driver output is up to VDD rail. The measurable on-resistance R_{OH} in steady state is the conduction resistance of PM1. NM1 provides a narrow instant peak sourcing current up to 4A to eliminate the turn on time and delay. During the output turn on transition, the equivalent hybrid pull on transient resistance is $1.5R_{OL}$, which is much lower than the DC measured R_{OH}.

The N-type MOSFET NM2 composes the output stage pull down structure; the R_{OL} is the DC measurement and represents the pull down impedance. The output stage of SCT52243 provides rail-to-rail operation, and is able to supply 4A sourcing and 4A sinking peak current. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. The outputs of the dual channel drivers are designed to withstand 500-mA reverse current without either damaging the device or logic malfunction.

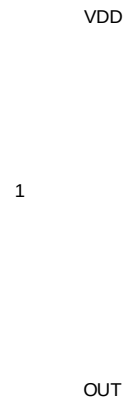


Figure 12. SCT52243 Output Stage

Stackable Output

The SCT52243 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. By using SCT52243, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA- and INB-. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA- and INB-, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA- and INB- input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us.

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Typical Application

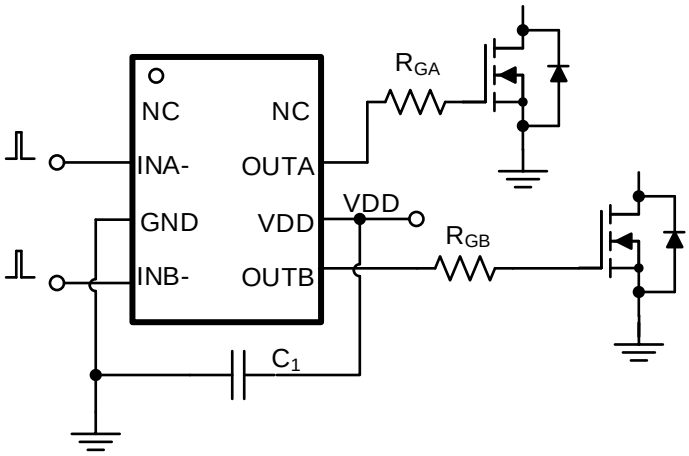


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52243 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52243 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52243 is:

(1)

Where

V_{DD} is supply voltage
C_{Load} is the output capacitance
F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52243 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

Q_g is the gate charge of the power device
f_{SW} is the switching frequency
V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Where

R_{OH} is the equivalent pull up resistance of SCT52243
R_{OL} is the pull down resistance of SCT52243
R

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms

Figure 17. VDD Power On

Figure 18. VDD Power Off

Figure 19. OUTA Switching Rise (Cload = 1nF)

Figure 20. OUTA Switching Fall (Cload = 1nF)

Figure 21. OUTB Switching Rise (Cload = 1nF)

Figure 22. OUTB Switching Fall (Cload = 1nF)

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Layout Guideline

The SCT52243 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52243 and Figure 23 is the layout example.

Put the SCT52243 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple. For the output stackable application, the driver input loop of two-channel input must be strictly symmetrical to ensure the input propagation delay is the same.

Star-point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane is to provide noise shielding and thermal dissipation as well.

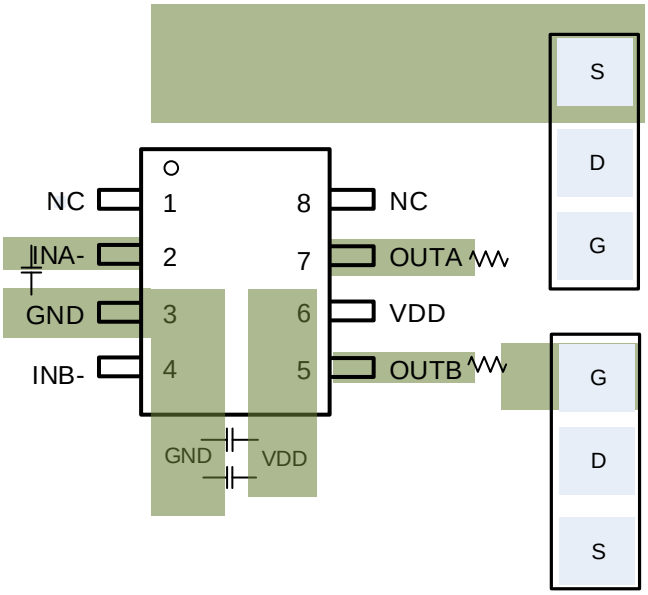


Figure 23. SCT52243 PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4).

(4)

where

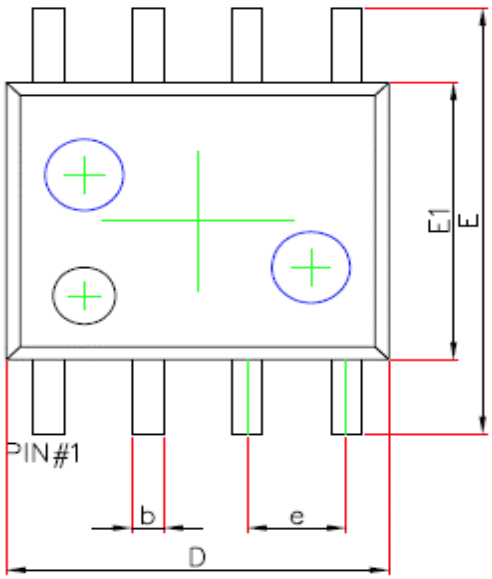
T_A is the maximum ambient temperature for the application.

R is the junction-to-ambient thermal resistance given in the Thermal Information table.

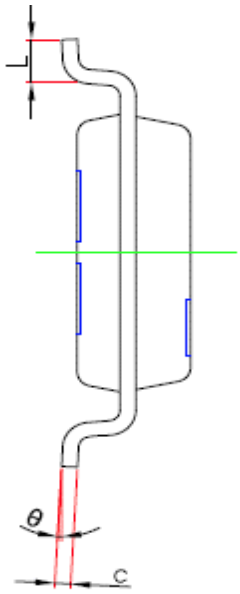
 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

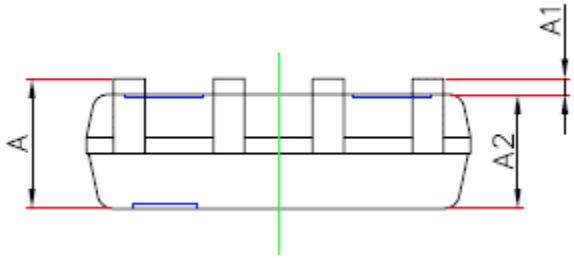
 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved



TOP VIEW



BOTTOM VIEW



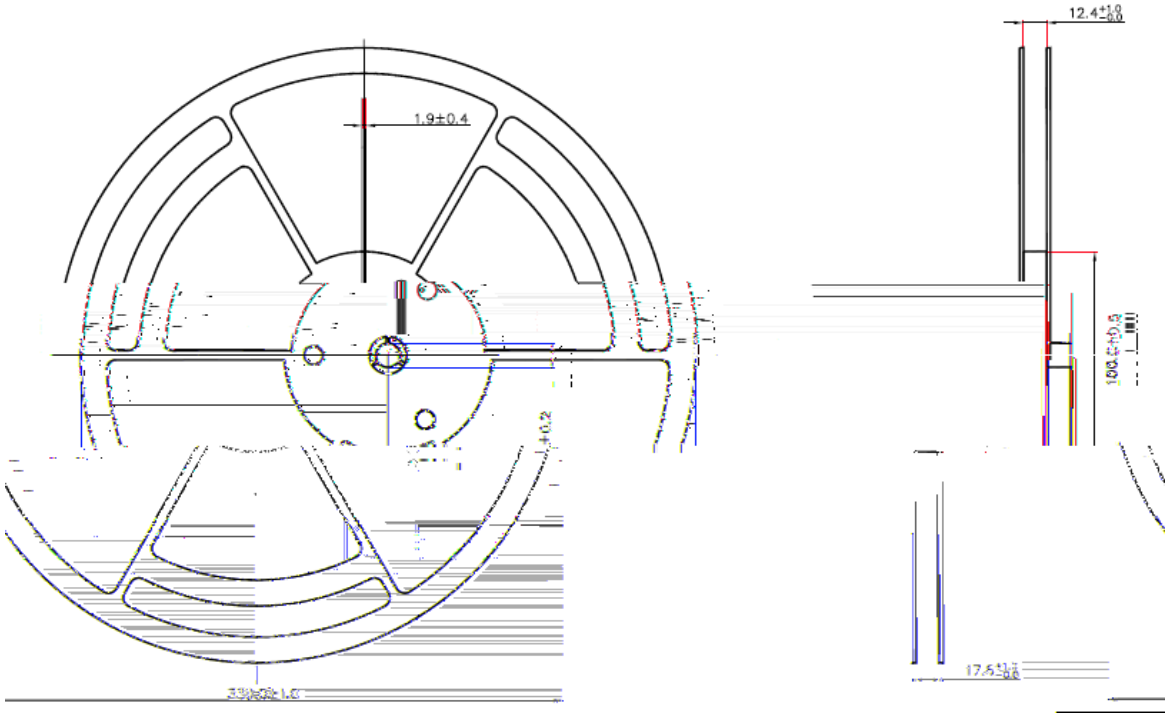
SIDE VIEW

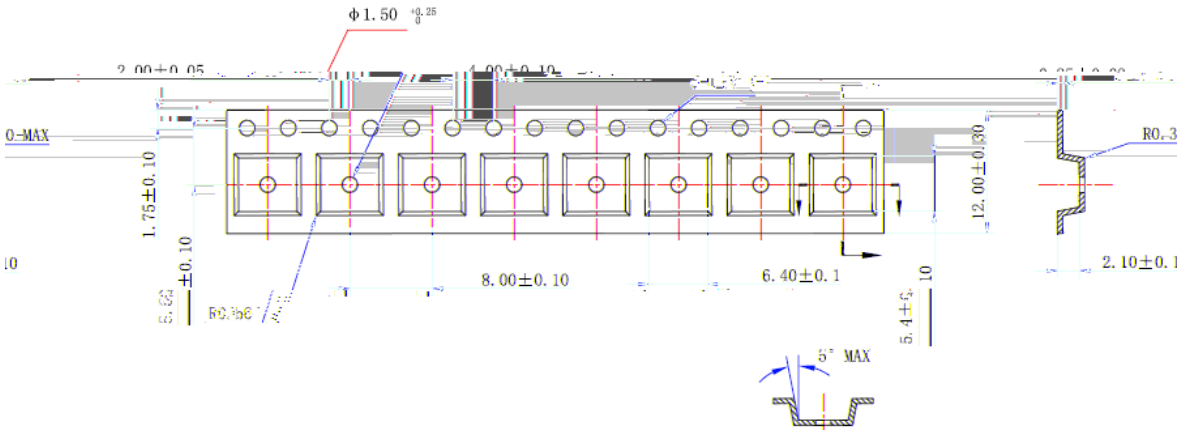
SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved





Feeding Direction

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved