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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Format adjustment, update ABS max, add EC table max limit

Revision 1.2: Correct package information in Page 16

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PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT52241STD	2241	SOP-8

1）For Tape & Reel, Add Suffix R (e.g. SCT52241STDR).

FC D D DI E

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ENA, ENB	-0.3	26	V
INA-, INB	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
VDD	-0.3	26	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

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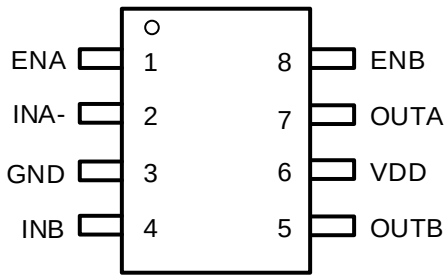
Top View: SOP-8pin Plastic



(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5		

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V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Supply current	EN=V_{DD}=3.5V, INA- =INB=3.5V		55		uA
		EN=V_{DD}=12V, INA- =INB= V_{DD}=12V		120		uA
INPUTS						
V_{INA-,INB_H}	Input logic high threshold Output low for inverting input Output high for non-inverting input			2.1	2.4	V
V_{INA-,INB_L}	Input logic low threshold Output high for inverting input Output low for non-inverting input		0.8	1		V
V_{IN_Hys}	Hysteresis			1.1		V
V_{ENA,ENB_H}	Enable logic high threshold			2.1	2.4	V
V_{ENA,ENB_L}	Enable logic low threshold		0.8	1		V
V_{EN_Hys}	Hysteresis			1.1		V
OUTPUTS						
V_{DD_VOH}	Output output high voltage	I_{OUT}= - 10mA			150	mV
V_{OL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF, F_{SW}=1kHz		4		A
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= - 10mA	5	9	18	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA	0.3	0.6	1.2	
Timing						
T_R	Output rising time	C_{Load}=1nF		8	20	ns
T_F	Output falling time	C_{Load}=1nF		8	20	ns
T_{D_IN}	Input to output propagation delay, Rising edge		7	13	25	ns
	Input to output propagation delay, Falling edge		7	13	25	ns
T_{M_IN}	Input to output delay matching					

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V_{IN}=12V, T_A= 25°C.

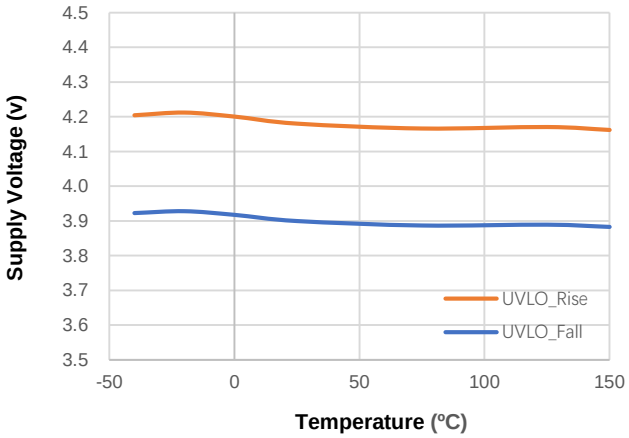

Figure 1. UVLO vs Temperature

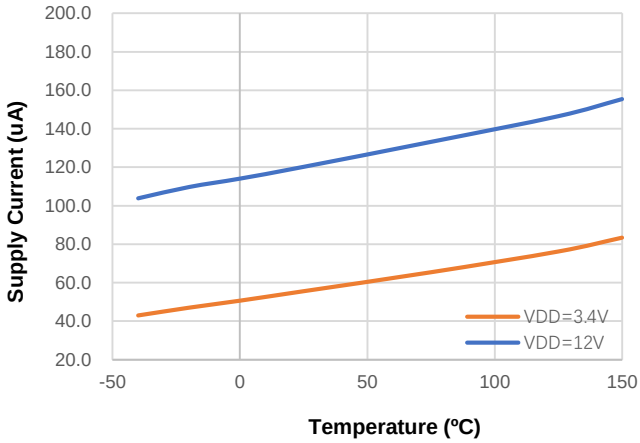

Figure 2. Supply current vs Temperature

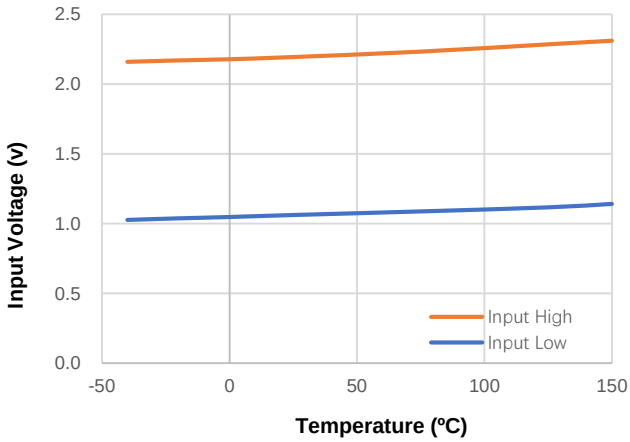

Figure 3. Input Threshold vs Temperature

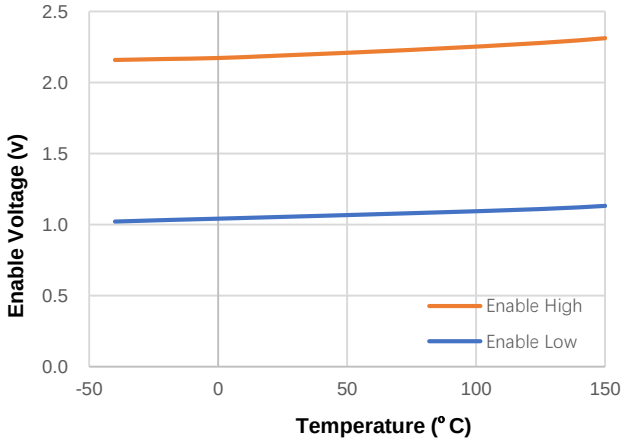

Figure 4. Enable Threshold vs Temperature

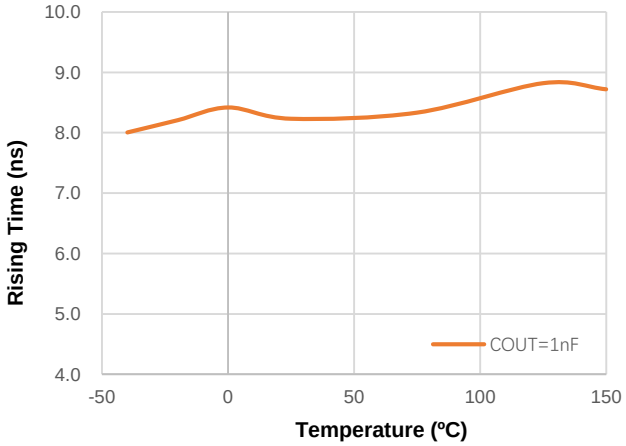

Figure 5 Output Rising Time vs Temperature

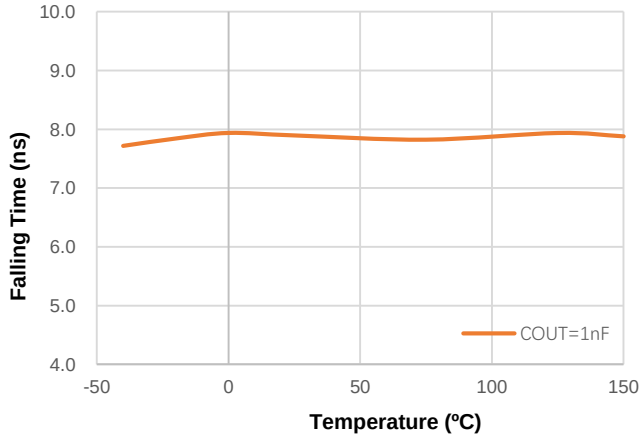

Figure 6. Output Falling Time vs Temperature

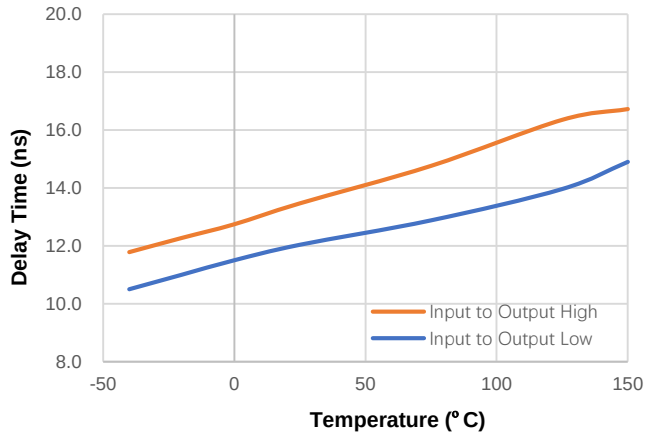

Figure 7. Input to Output Propagation Delay vs Temperature

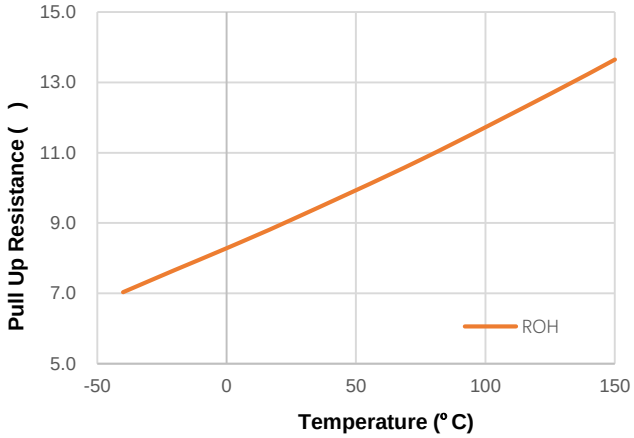

Figure 8. ROH vs Temperature

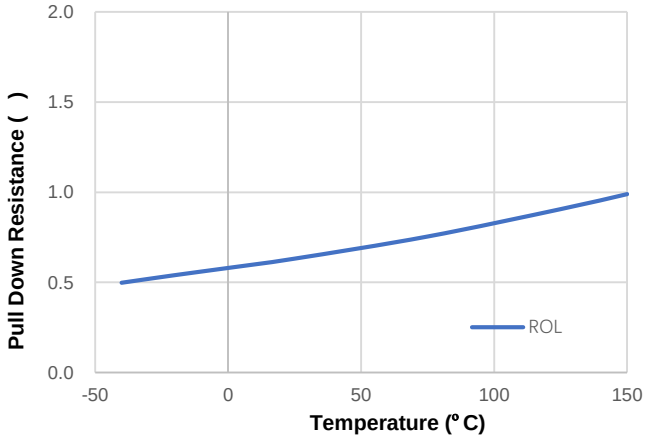

Figure 9. ROL vs Temperature

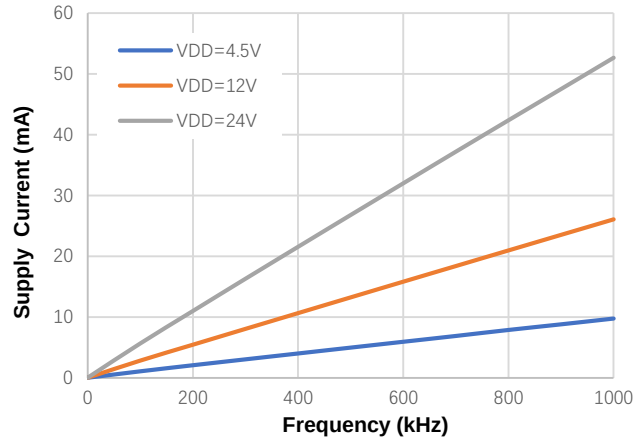

Figure 10. Operation Supply Current vs Frequency, C_{OUT}=1nF

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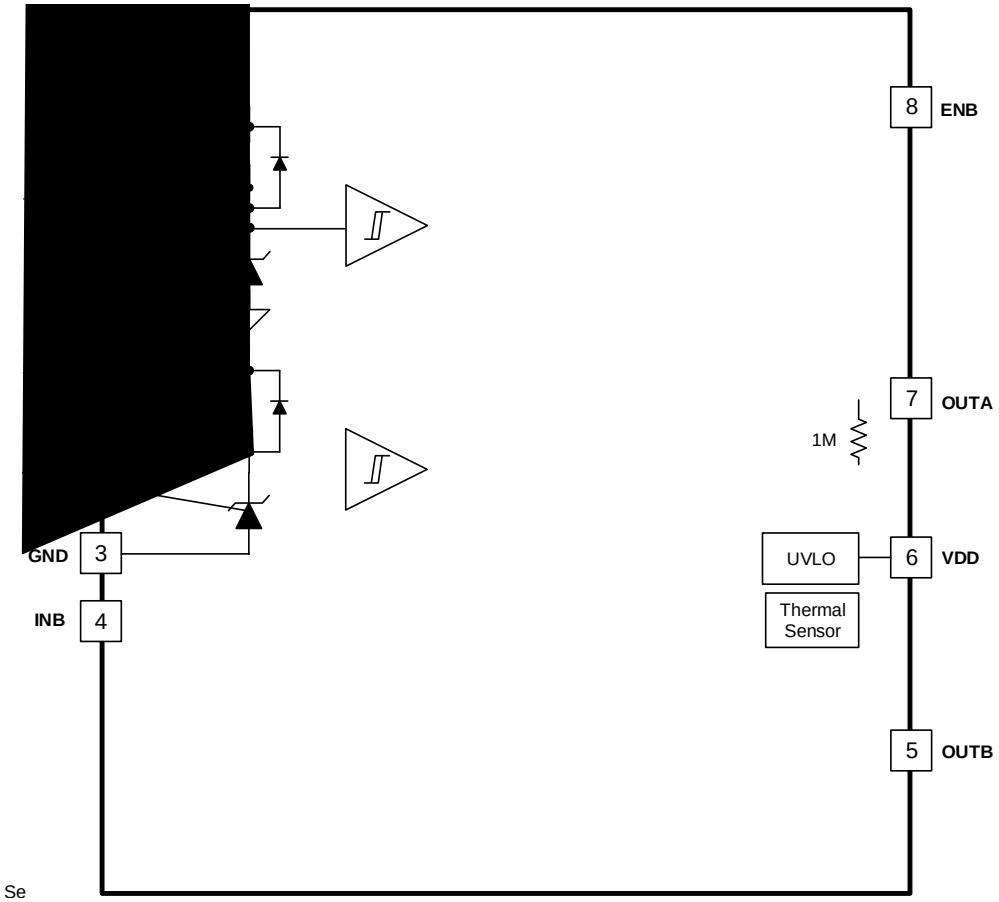

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Overview

The SCT52241 is a dual-channel high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52241 output stage robustness during switching load fast transition. The SCT52241 has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52241 Device Logic.

ENA	ENB	INA-	INB	OUTA	OUTB
H	H	L	L	H	L
H	H	L	H	H	H
H	H	H	L	L	L
H	H	H	H	L	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	H	L
Floating	Floating	L	H	H	H
Floating	Floating	H	L	L	L
Floating	Floating	H	H		

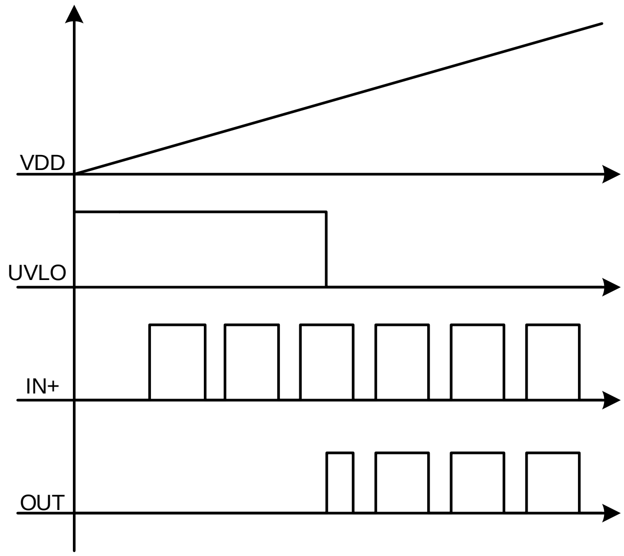

Figure 11. SCT52241 Non-inverting Output Vs VDD

Enable Function

SCT52241 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply voltage and is effectively controlled with logic signals from 3.3-V and 5-V microcontrollers. When applying a voltage higher than the high threshold (typical 2.1V) the pin, the SCT52241 enables all functions and starts gate driver operation. Driver operation is disabled when ENx voltage falls below its lower threshold (typical 1V). The ENx pins are internally pulled up to VDD with 400k pullup resistors. Hence, the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not required.

Input Stage

The input of SCT52241 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. SCT52241 also features tight control of the input pin threshold voltage that ensures stable operation across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

Output Stage

The SCT52241 output stage features the pull up structure with P-type MOSFET PM1 and N-type MOSFET NM1 in parallel, as shown in Figure 12. PM1 provides the pull up capability when OUT approaches VDD and the NM1 holds off state, which guarantees the driver output is up to VDD rail. The measurable on-resistance R_{OH} in steady state is the conduction resistance of PM1. NM1 provides a narrow instant peak sourcing current up to 4A to eliminate the turn on time and delay. During the output turn on transition, the equivalent hybrid pull on transient resistance is $1.5R_{OL}$, which is much lower than the DC measured R_{OH}.

The N-type MOSFET NM2 composes the output stage pull down structure; the R_{OL} is the DC measurement and

rep(e)sent(NM2)-W*nBT2 9.96 Tf1 0 0 1 54 322.61 Tm0 g0 G[(T)-15(he)4( )-22(i)5(np)4(u)-9(t)-310 G00000©1 eBT.784reW000

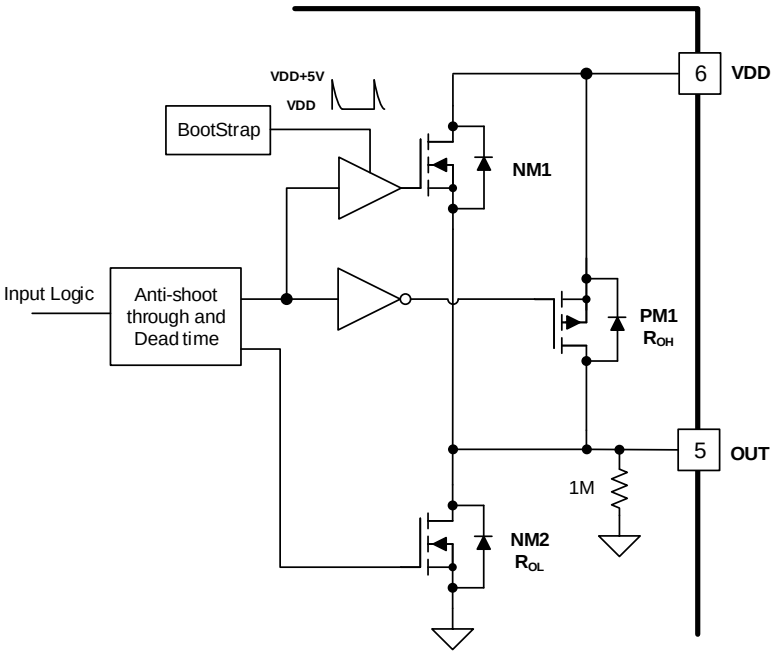

Figure 12. SCT52241 Output Stage

Thermal Shutdown

Once the junction temperature in the SCT52241 exceeds 170° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Where

- R_{OH} is the equivalent pull up resistance of SCT52241
- R_{OL} is the pull down resistance of SCT52241
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

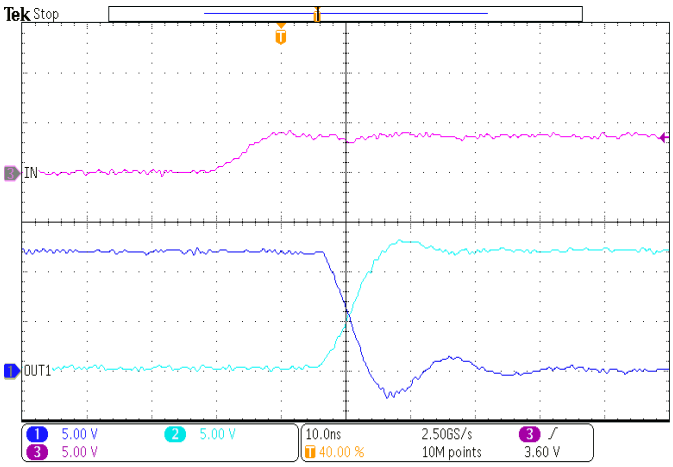

Figure 17. Driver Switching ON

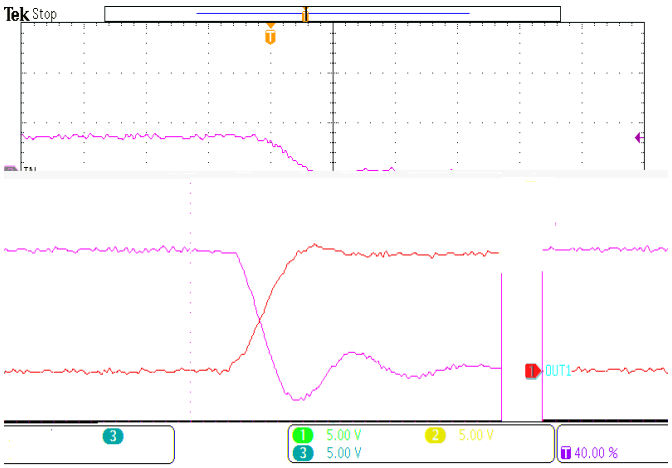

Figure 18. Driver Switching OFF

Layout Guideline

The SCT52241 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52241 and Figure 19 is the layout example.

Put the SCT52241 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple.

Star-point grounding is recommend to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane is to provide noise shielding and thermal dissipation as well.

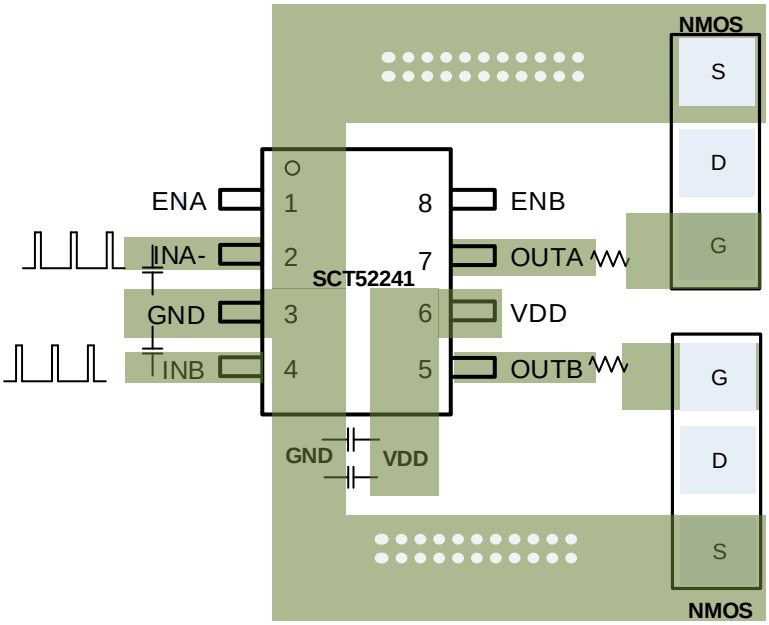

Figure 19. SCT52241 PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4).

(4)

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, and

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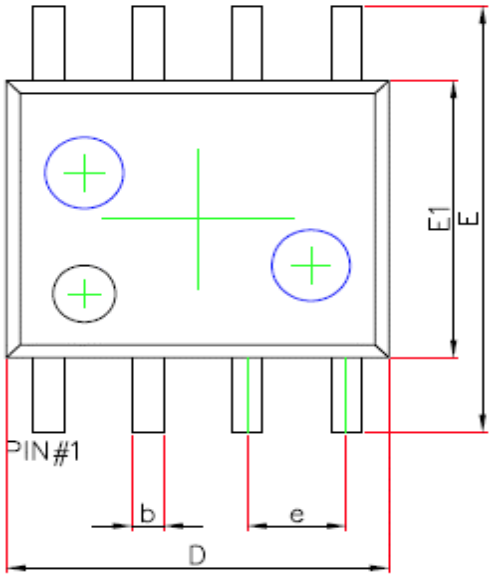
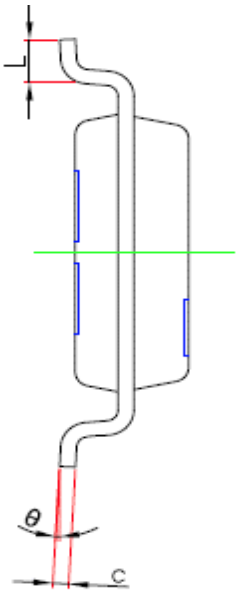
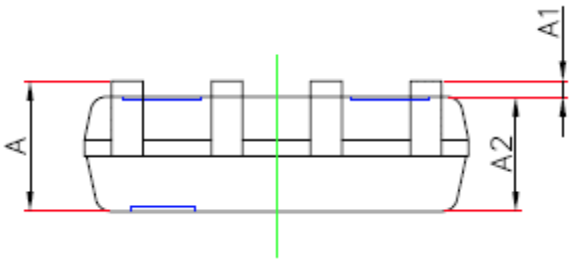


TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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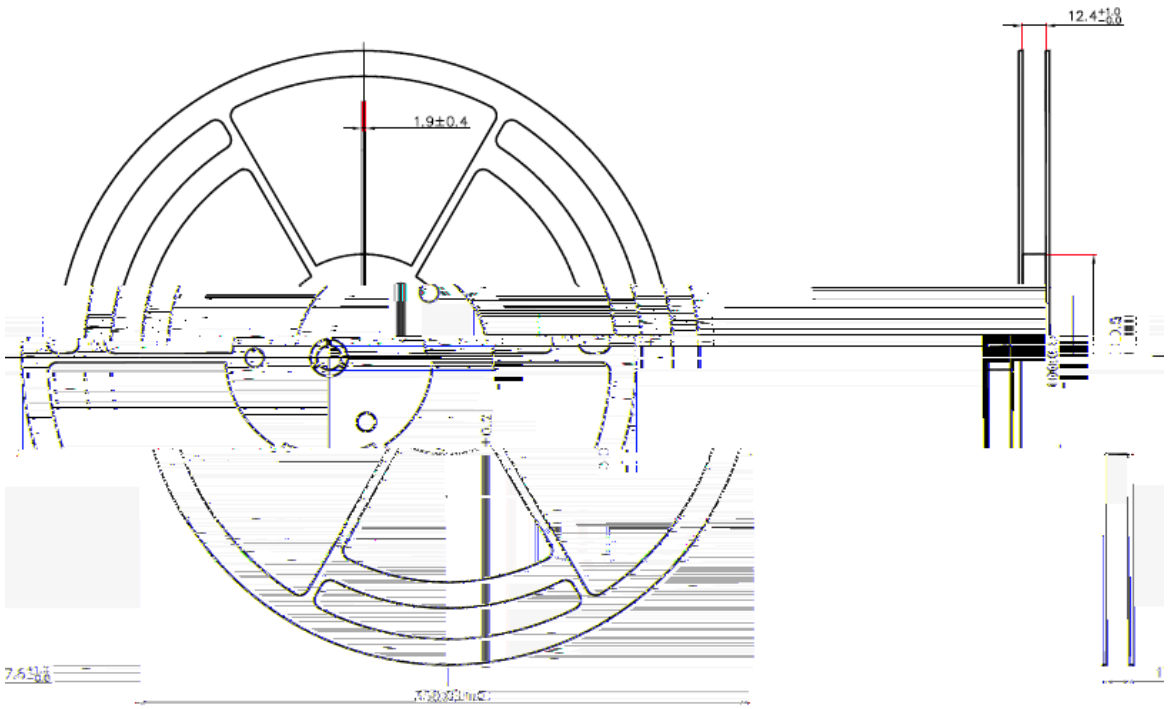

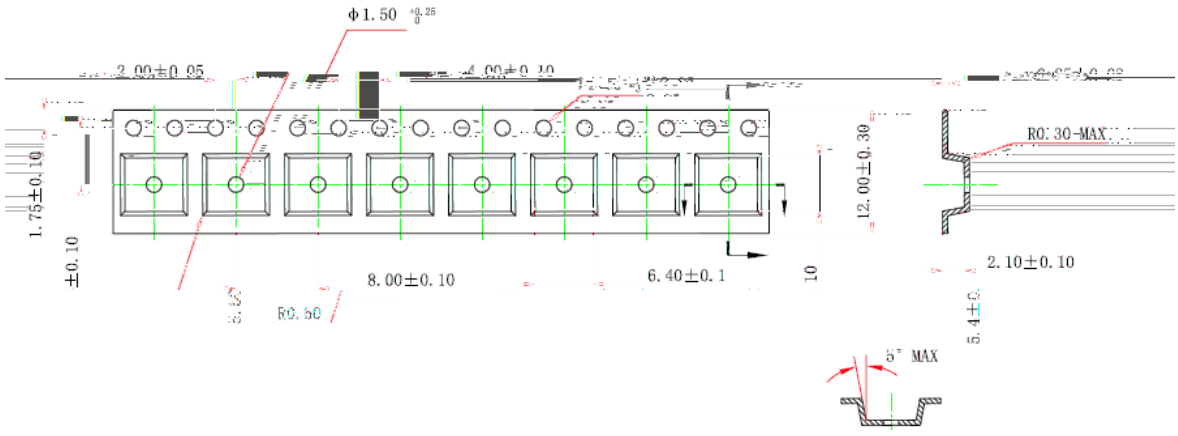

Feeding Direction

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Single Channel, Non-Inverting MOSFET Gate Drive
Typical Application