V Vin, 3A Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Voltage: 4.2-17V
- 3A Continuous Output Current with Integrated 90mΩ/54mΩ FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 135uA
- Cycle-by-Cycle Current Limiting
- Internal 2.5ms Soft-Start Limits the inrush current
- Fixed 750kHz Switching Frequency
- Input Under-Voltage Lockout
- Power save mode at light load
- Over-Temperature Protection
- Available in a TSOT23-6 Package

APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

DESCRIPTION

The SCT2230C is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 3A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

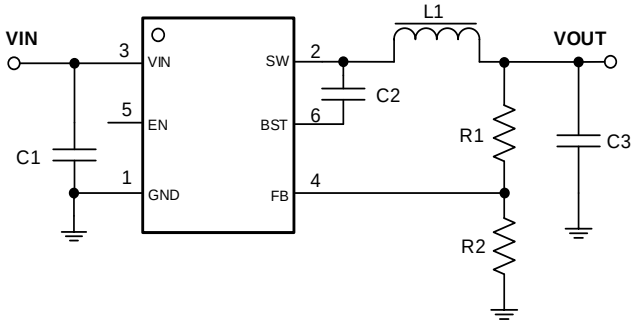
With 750 kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2230C adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

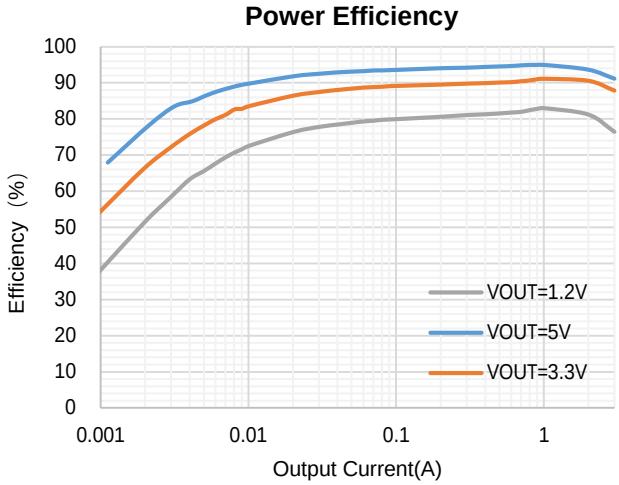
The SCT2230C operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2230C requires a minimal number of external components and is available in a space-saving TSOT23-6 package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev 1.0: Released to Market

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2230CTVB	230C	TSOT23-6L

* (1) FOR TAPE & REEL, ADD SUFFIX R (E.G. SCT2230CTVBR).

ABSOLUTE MAXIMUM RATING

Over operating free-air temperature unless otherwise noted(1)

SYMBOL	RATING	UNIT
V_{IN}	-0.3 to 18	V
V_{SW}	-1 to VIN+0.3	V
V_{BST}	V_{SW}-0.3 to V_{SW}+6	V
V_{FB}	-0.3 to 6.5	V
V_{EN}	-0.3 to 6.5	V
T_J	-40 to 125	C

PIN CONFIGURATION

TSOT23-6 Top View
(2.8mm x 2.8mm)

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
GND	1	Power ground. Must be soldered directly to ground plane.
SW	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	5	Enable logic input. Floating the pin enables the device. The device has precision enable thresholds 1.2V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	17	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	88	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	12	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2230C are mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2230C. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.9 300	4.15	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1.5	5	uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=12V. BST-SW=5V		135		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.2	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN}	Enable pin input current	EN=1V	1	1.5	2	uA
		EN=1.5V		6.8		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			90		mΩ
R_{DSON_L}	Low side FET on-resistance			54		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		0.78	0.8	0.82	V
Current Limit						
I_{LIM_LSD}	LSD valley current limit		3.2	3.7	4.2	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V		750		kHz
t_{ON_MIN}	Minimum on-time*			90		ns
t_{OFF_MIN}	Minimum off-time			220		ns
Soft Start Time						
t_{SS}	Internal soft-start time			2.5		ms
Protection						
T_{SD}	Thermal shutdown threshold* Hysteresis	T_J rising		160 20		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

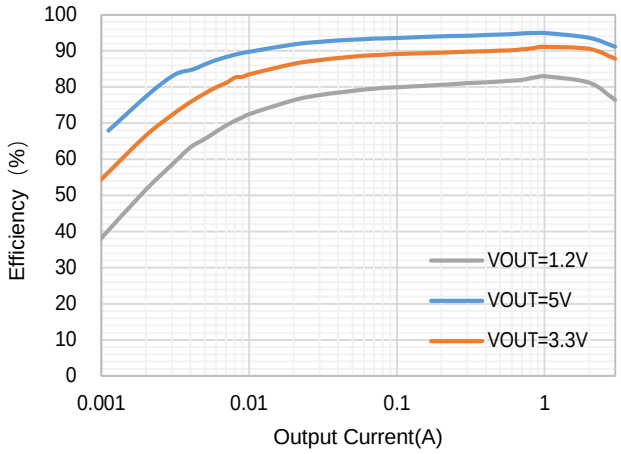


Figure 1. SCT2230C Efficiency, Vin=12V

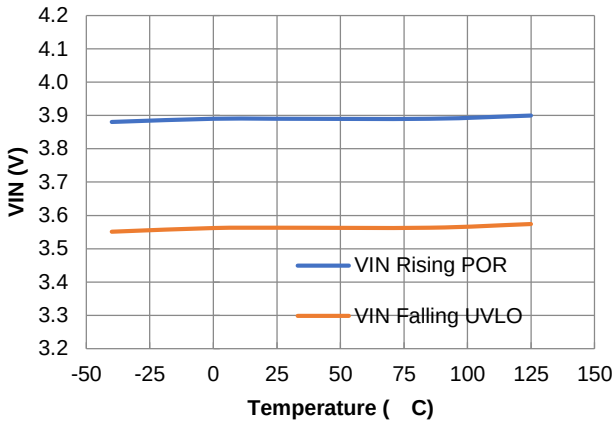


Figure 2. UVLO Vs. Temperature

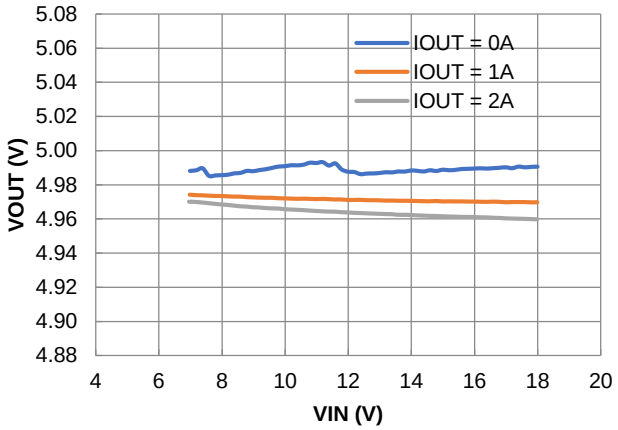


Figure 3. Line Regulation

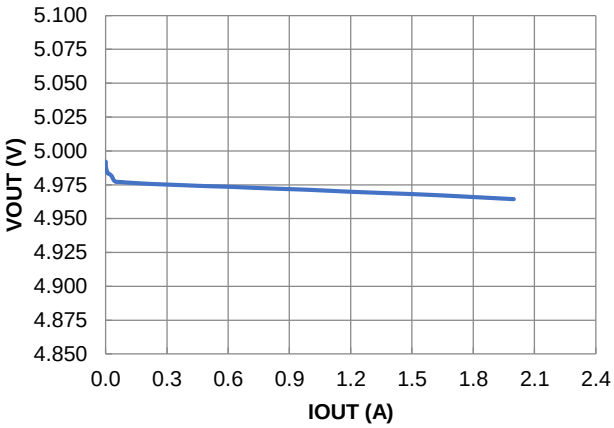


Figure 4. Load Regulation

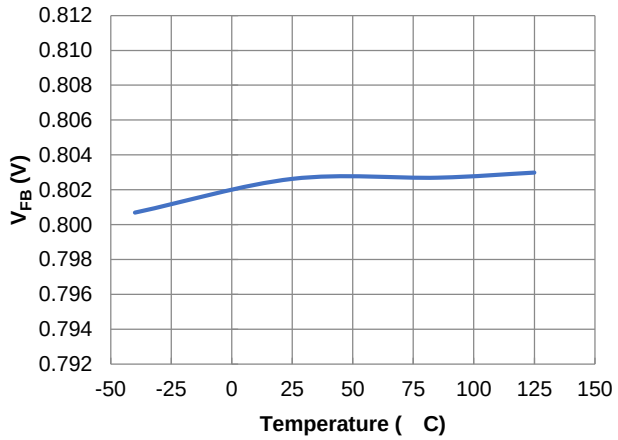


Figure 5. Feedback Voltage vs. Temperature

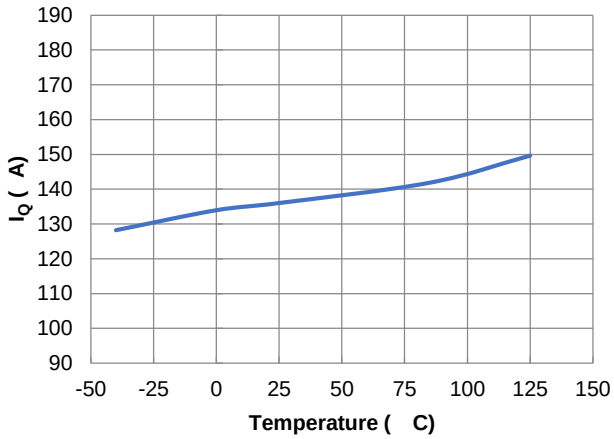
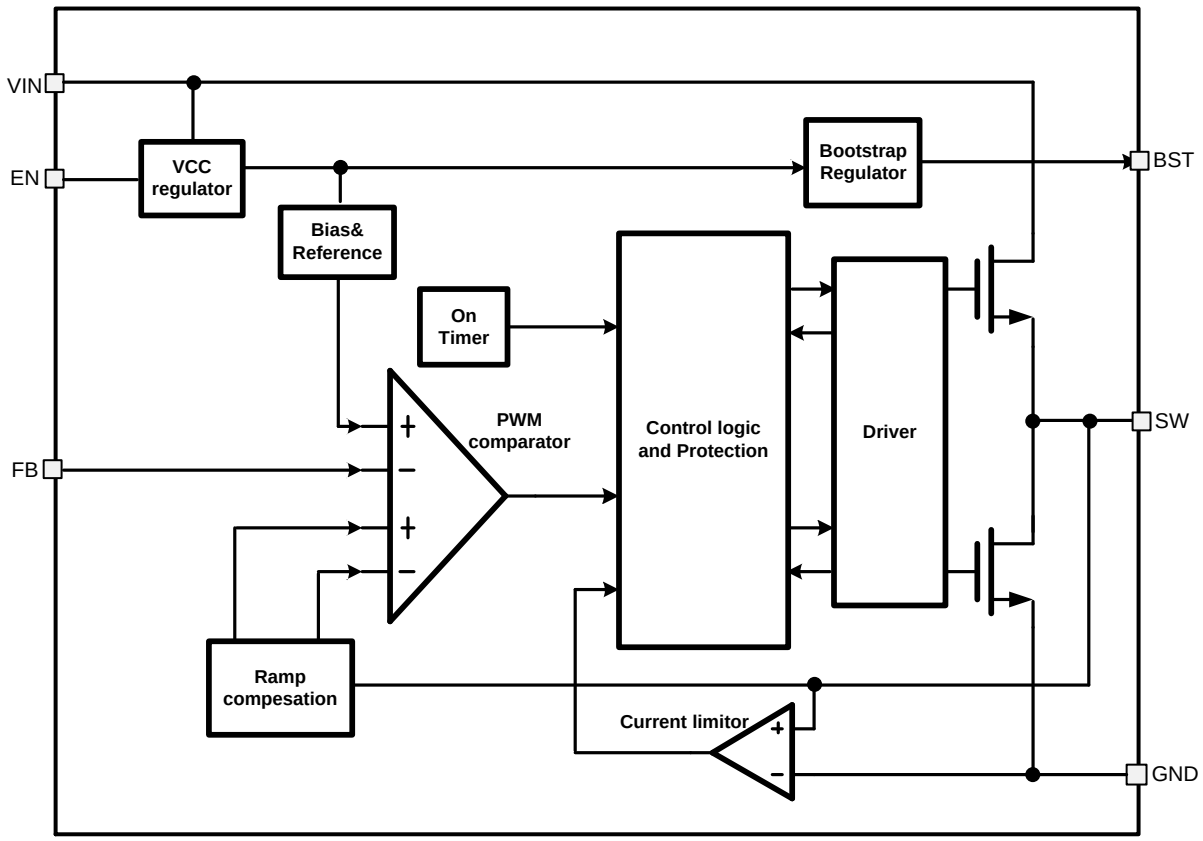


Figure 6. Quiescent Current vs. Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Adaptive On-time Control

The SCT2230C device is 4.2-17V input, 3A output, synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2230C turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2230C turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} \quad \frac{V_{OUT}}{V_{IN} \quad f_S} \tag{1}$$

Where:

VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 200ns typical.

Pulse Frequency Modulation (PFM)

The SCT2230C is designed with Pulse Frequency Modulation (PFM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.8V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing VOUT ripple at light load condition. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} \quad \frac{V_{IN} \quad V_{OUT}}{2L} \quad T_{ON} \tag{2}$$

Where:

TON is on-time

VIN Power

The SCT2230C is designed to operate from an input voltage supply range between 4.2V to 17V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2230C Under Voltage Lock Out (UVLO) default startup threshold is typical 3.9V with VIN rising and shutdown threshold is 3.6V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2230C enables all functions and the device starts soft-start phase. The SCT2230C has the built in 2.5ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 5.3uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (3) and (4).

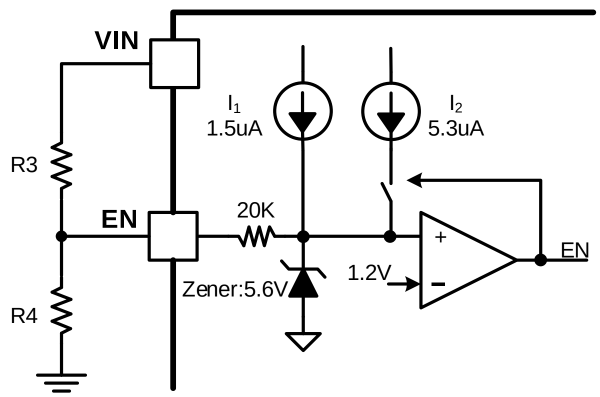


Figure 7. Adjustable VIN UVLO

(3)

(4)

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=5.3uA
V_{ENR}=1.2V
V_{EMF}=1.1V

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will dropped below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2230C exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Output Feedback Resistor Divider Selection

The SCT2230C features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (8) to calculate the resistor divider values.

(8)

Table 2. Recommended Component Selections

Output Voltage (V)			L (µH)	C1 (µF)	C2 (µF)	C3 (nF)
1.2	4.99	10	1.5	10	2 x 22	100
	8.66	10	1.5	10		100

Application Waveforms

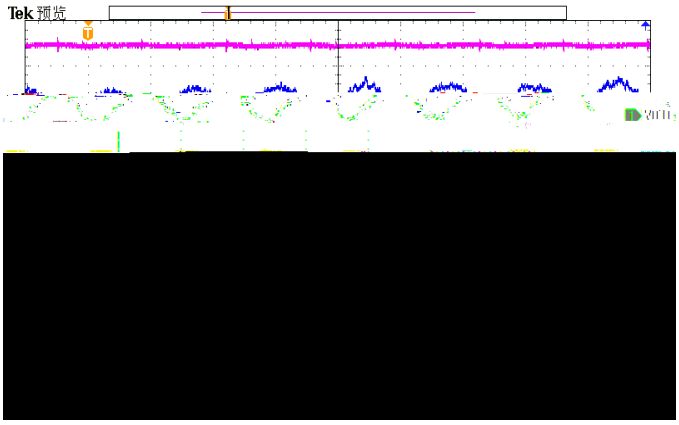


Figure 9. SW node waveform and Output Ripple
VIN=12V, IOUT=3A

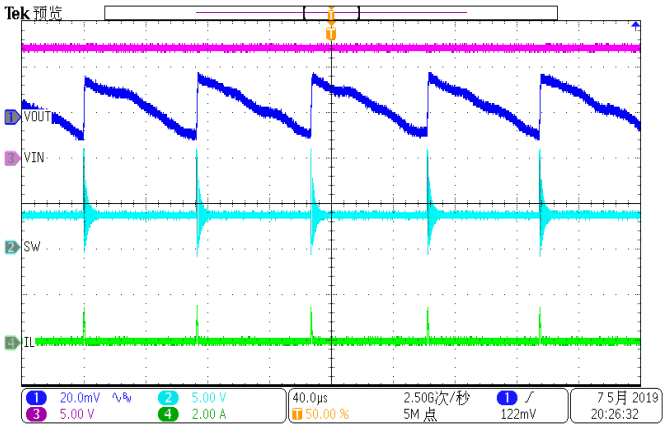


Figure 10. SW node Waveform and Output Ripple
VIN=12V, IOUT=10mA

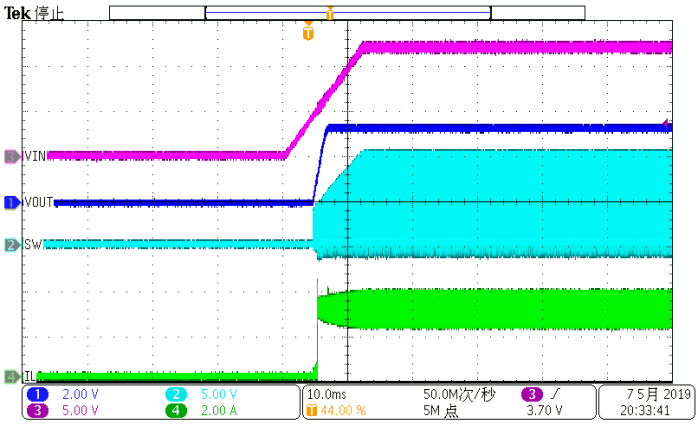


Figure 11. Power Up
VIN=12V, VOUT=3.3V, IOUT=3A

Figure 12. Power Down
VIN=12V, VOUT=3.3V, IOUT=3A

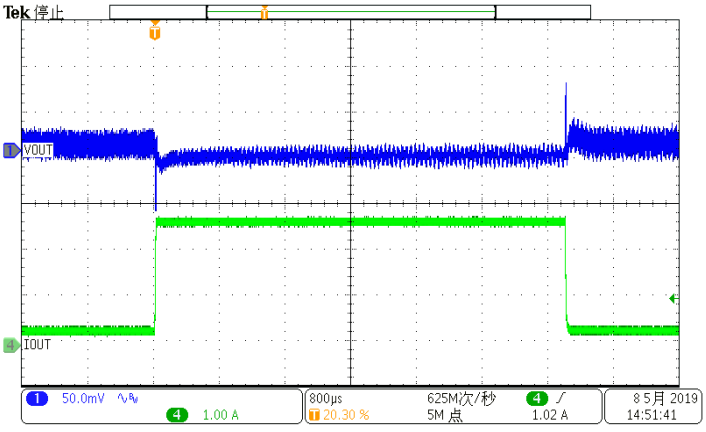


Figure 13. Load Transient
VOUT=3.3V, IOUT=0.3A to 2.7A, SR=250mA/us

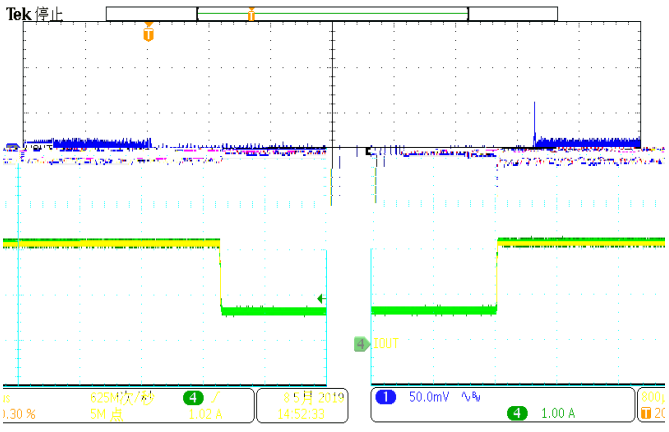


Figure 14. Load Transient
VOUT=3.3V, IOUT=0.75A to 2.25A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15 is the recommended PCB layout of SCT2230C.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

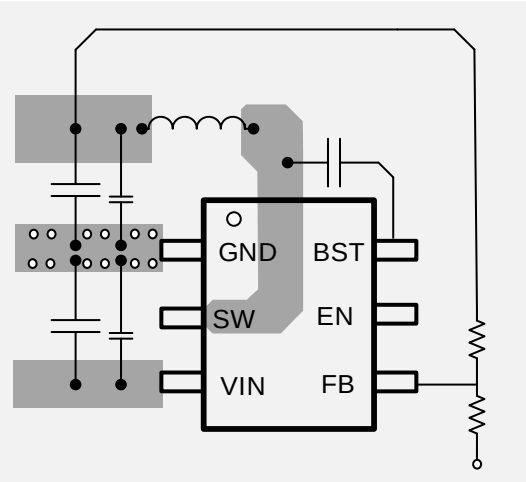


Figure 15. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

(9)

where

T_A is the maximum ambient temperature for the application.
$R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

PACKAGE INFORMATION

TSOT23-6 TOP VIEW

TSOT23-6 BOTTOM VIEW

TSOT23-6 SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.