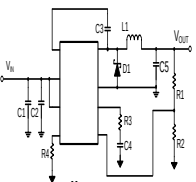


я ` + Ï 2 a MMM

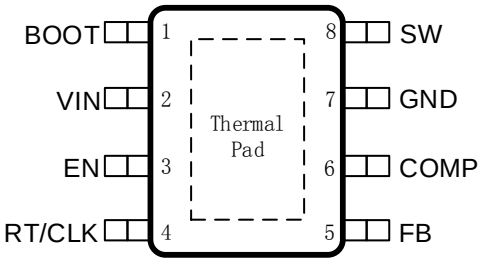
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Production

SCT2650STE	2650	ESOP-8

1) For Tape & Reel, Add Suffix R (e.g. SCT2650STER)

Over operating free-air temperature unless otherwise noted(1)

VIN, EN	-0.3	65	V
BOOT	-0.3	72	V
SW	-1	65	V
BOOT-SW	-0.3	6	V
COMP, FB, RT/CLK	-0.3	6	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C



(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.2V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT/CLK	4	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	

SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	60	V
V_{OUT}	Output voltage range	0.8	57	V
T_J	Operating junction temperature	-40	150	°C

V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	+1	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

	Junction-to-ambient thermal resistance (standard board)	42	°C/W
	Junction-to-top characterization parameter	5.9	

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		4.5		60	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		4.2	4.4	V
	Hysteresis			320		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		2	5	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		175		

V_{COMP_H}	COMP high clamp		2.25	V
V_{COMP_L}	COMP low clamp		0.47	V

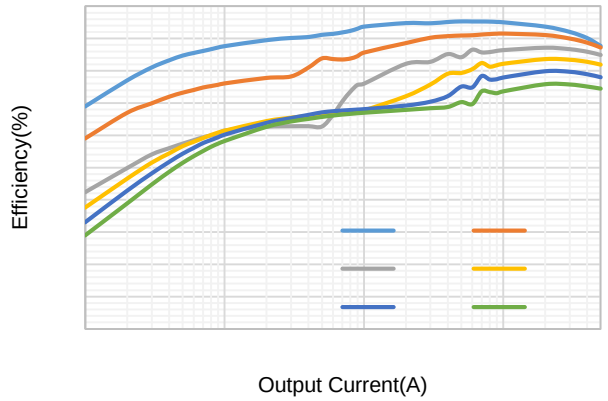


Figure 2. Efficiency vs Load Current, Vout=5V

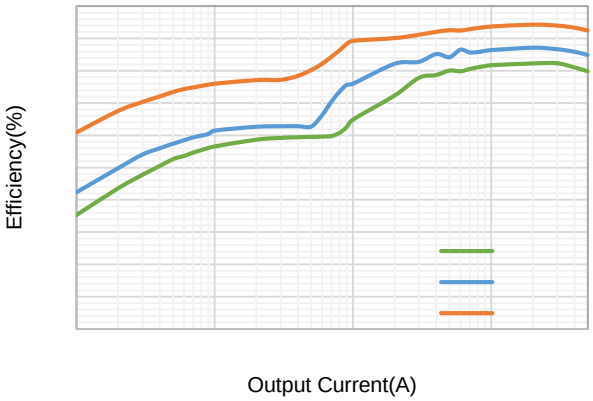


Figure 3. Efficiency vs Load Current, Vin=24V

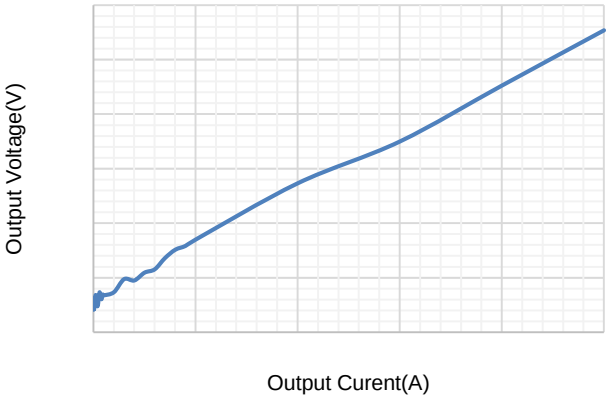


Figure 4. Load Regulation, Vin=24V, Vout=3.3V

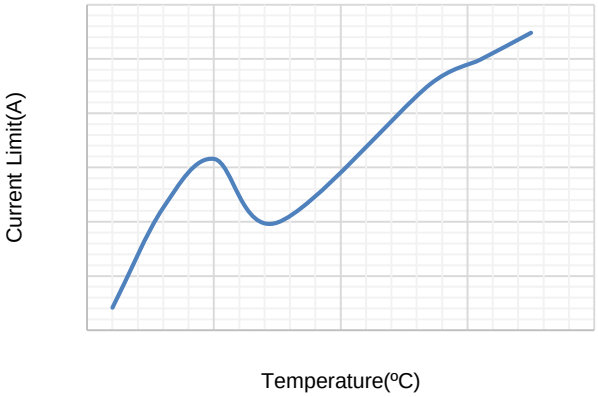


Figure 5. Current Limit VS Temperature

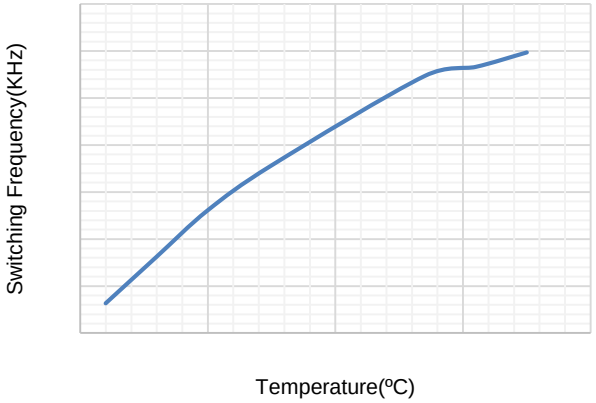


Figure 6. Switching Frequency VS Temperature

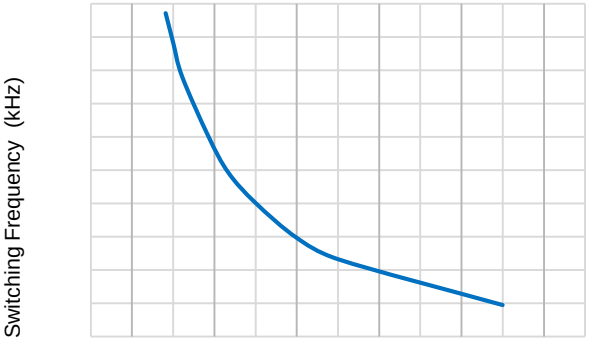


Figure 7. Switching Frequency vs RT Resistor

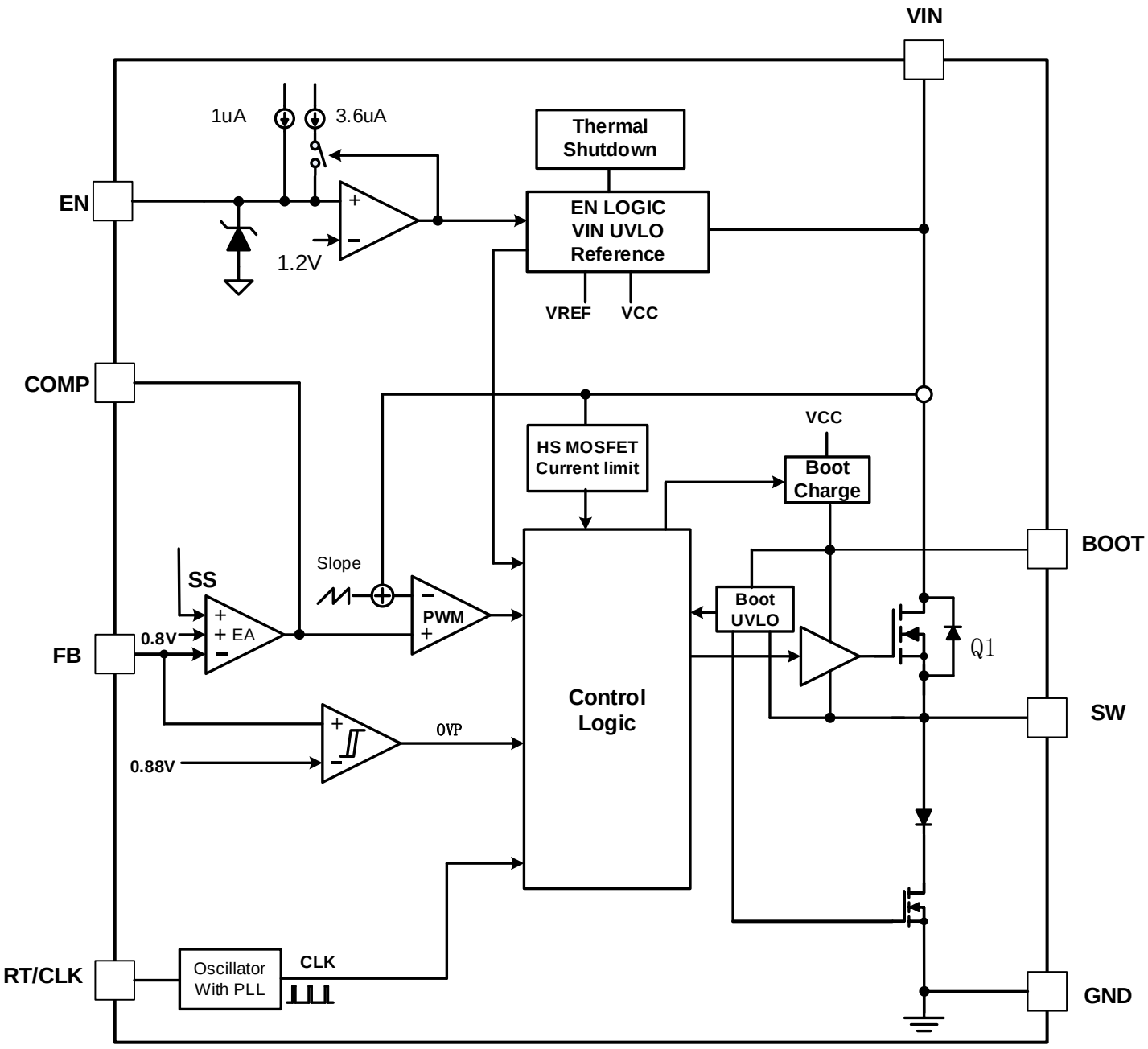


Figure 8. Functional Block Diagram

The SCT2650 is a 4.5V-60V input, 5A output, buck converter with integrated 80mΩ Rdson high-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external loop compensation design.

The switching frequency is programmable from 100kHz to 1.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT2650 features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 175uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2650 has a default input start-up voltage of 4.2V with 320mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2650 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

The SCT2650 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2650 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (470mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 200mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 175uA during skipping period with no switching to improve efficiency further.

The SCT2650 is enabled when the VIN pin voltage rises above 4.2V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 3.9V or when the EN pin voltage is below 1.2V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

(1)

(2)

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

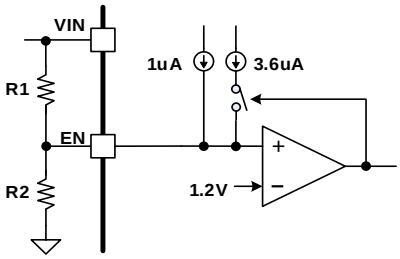


Figure 9. System UVLO by enable divide

The SCT2650 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

(3)

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

The SCT2650 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.2V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

The switching frequency of the SCT2650 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 1.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

where, fsw is switching clock frequency

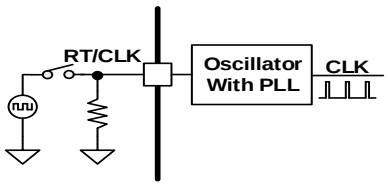


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100KHz to 1.2MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.52V and hysteresis of 230mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.29V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2650 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.52V. When the voltage from BOOT to SW drops below 2.29V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.52V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2650 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

The SCT2650 implements over current protection with fold back current limit. The SCT2650 cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 2.25V typical.

The SCT2650 implements frequency foldback to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The SCT2650 uses a digital frequency foldback to enable synchronization
u / to anæexternal clock duri

inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT}. The selected operating frequency must not exceed the calculated value.

(5)

where

: Limited average current

: Inductor DC resistance

_ : Maximum input voltage

_ : Output voltage during short

: Diode voltage drop

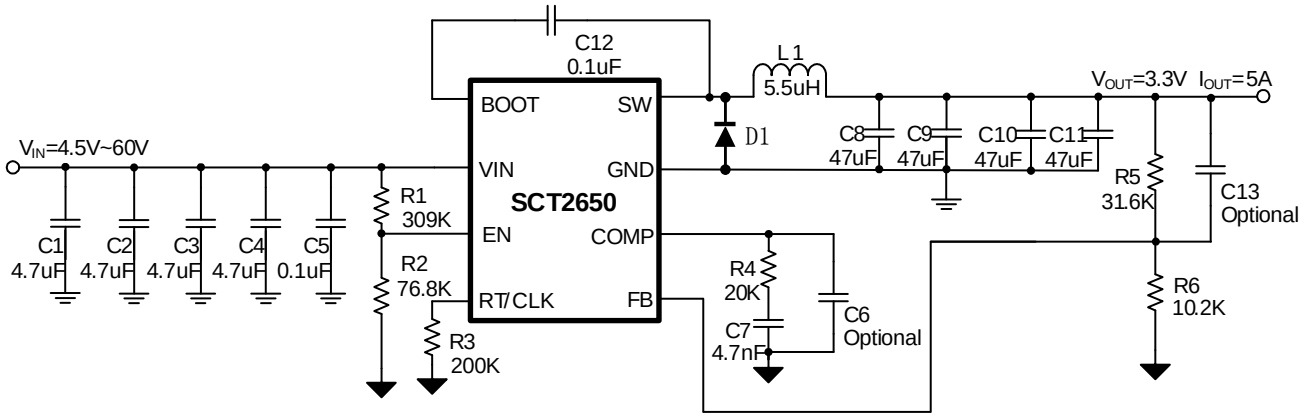
: Integrated high side FET on resistance

_ : Controllable minimum on time

: Frequency divide equals (1,2,4 or 8)

The SCT2650 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

The SCT2650 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160C, the device restarts with internal soft start phase.



Input Voltage	24V Normal 4.5V to 60V
Output Voltage	3.3V
Maximum Output Current	5A
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	16.5mV
Transient Response 1.25A to 3.75A load step	ΔVout = 135mV
Start Input Voltage (rising VIN)	5.76V
Stop Input Voltage (falling VIN)	4.66V

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 6 to calculate R5.

(6)

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ
36V	442 KΩ	10.2 KΩ
48V	604 KΩ	10.2 KΩ

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The 130ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 500 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 7, or determined from Figure 7.

(7)

where:

- f_{SW} is the desired switching frequency

200 KHz	500 KΩ
330 KHz	301 KΩ
500 KHz	200 KΩ
1100 KHz	90.9 KΩ

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.76V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.66 V (stop or disable). Use Equation 8 and Equation 9 to calculate the values 309 kΩ and 76.8 kΩ of R_1 and R_2 resistors.

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 17 and the maximum input voltage ripple occurs at 50% duty cycle.

(17)

For this example, four 4.7μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 18 desired.

(18)

Where

- Δ is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 47μF ceramic output capacitors work for most applications.

The SCT2650 employs peak current mode control for easy compensation and fast transient response. An external network comprising resister R4, ceramic capacitors C7 and optional C6 connected to the COMP pin is used for the loop compensation. The equation 19 shows the close-loop small signal transfer function.

The DC voltage gain of the loop is given by equation 20.

(20)

The system has two noteworthy poles: one is due to the compensation capacitor C7 and the error amplifier output resistor. The other is caused by the output capacitor and the load resistor. These poles as located at:

(21)

(22)

where

- R_{OEA} is error amplifier output resistor
- G_{EA} is Error amplifier trans-conductance, 300uS typically
- R_{LOAD} is equivalent load resistor

The system has one zero of importance from R4 and C7. fz1 is used to counteract the fp2, and fz1 located at:

(23)

The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the capacitance of the output capacitor is calculated by Equation 24.

(24)

In this case, a third pole set by the optional compensation capacitor C6 and the compensation resistor R4 is used to compensates the effect of the ESR zero. This pole is calculated by Equation 25.

(25)

The crossover frequency of converter is shown in Equation 26.

(26)

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R4 with Equation 27 once crossover frequency is selected.

(27)

Then calculate C7 by placing a compensation zero at or before the output stage pole.

(28)

Determine if the optional compensation capacitor C6 is required. Generally, it is required if the ESR zero f_{Z2} is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C6 can be calculated with Equation 29.

(29)

Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions not list in Table 3, customers can use Equation 27-Equation 29 to optimize the compensation components.

The SCT2650 can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.

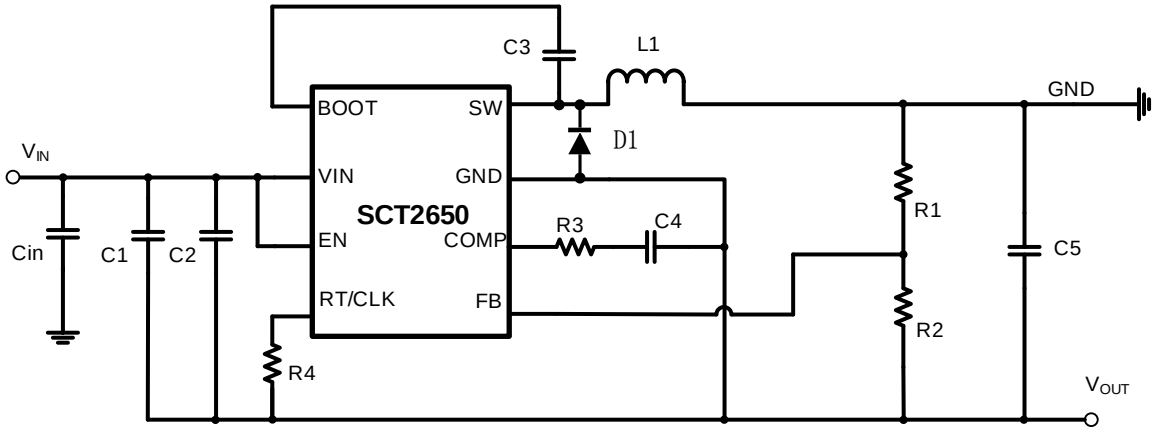


Figure 12. SCT2650 Inverting Power Supply

Vin=24V, Vout=3.3V, unless otherwise noted

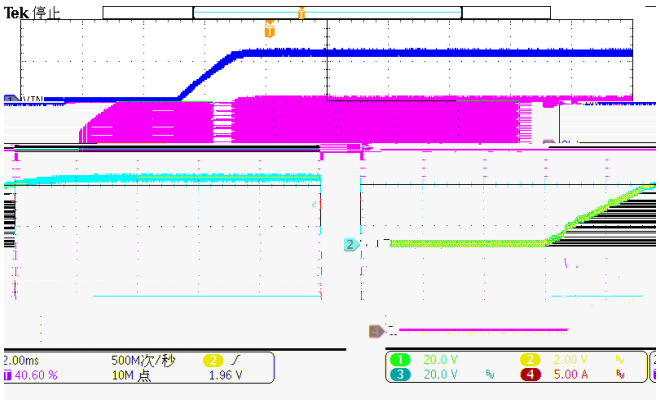


Figure 13. Power up(Iload=5A)

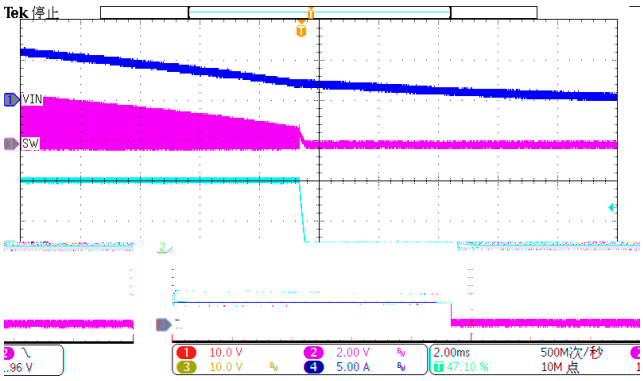


Figure 14. Power down(Iload=3.5A)

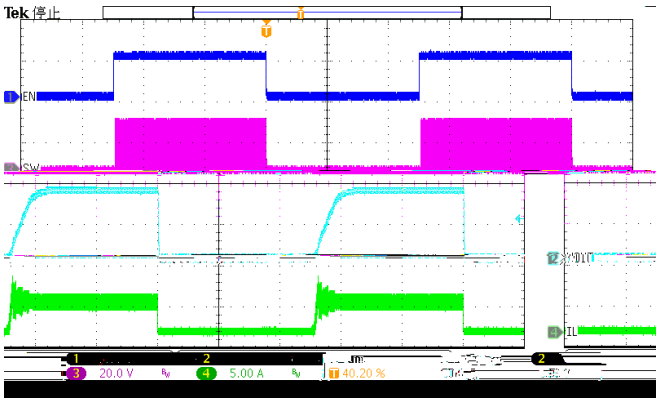


Figure 15.EN toggle (Iload=3.5A)

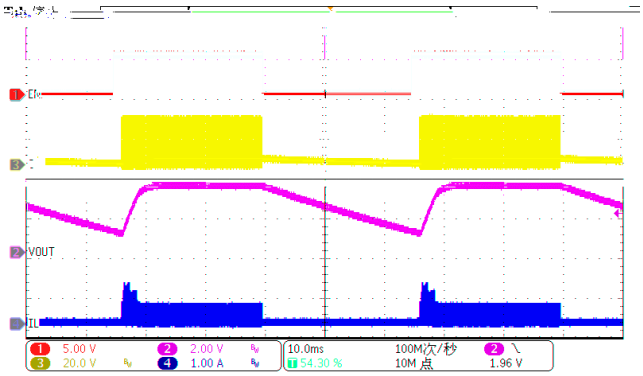


Figure 16. EN toggle (Iload=20mA)

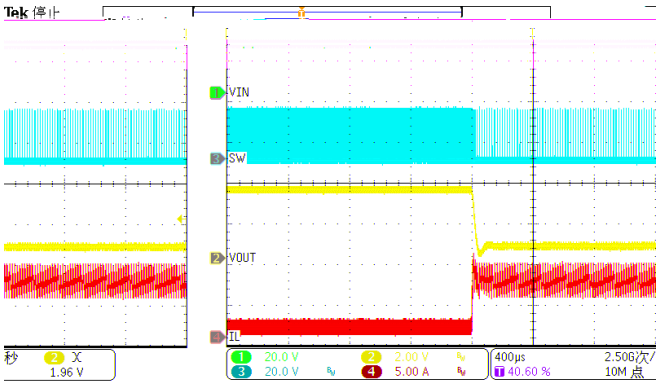


Figure 17. Over Current Protection(1A to hard short)

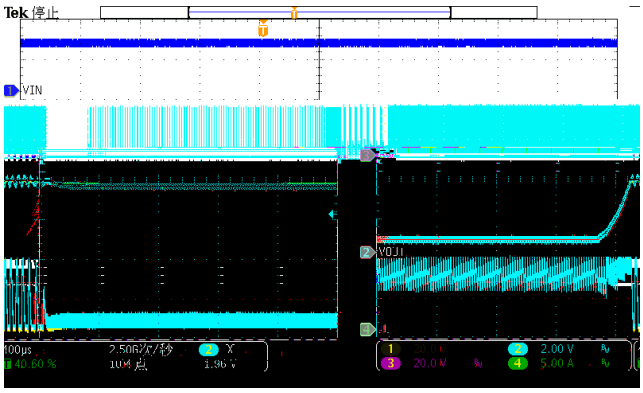


Figure 18. Over Current Release (hard short to 1A)

Vin=24V, Vout=3.3V, unless otherwise noted

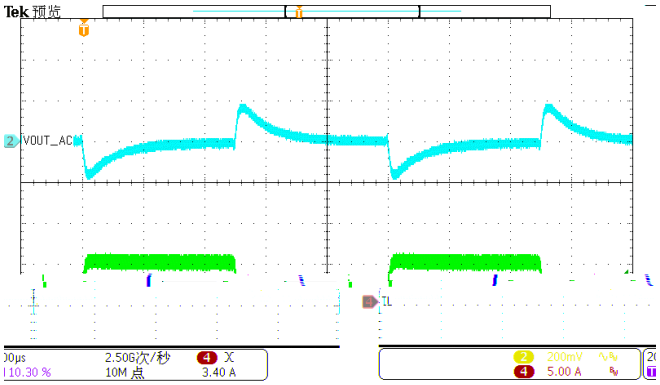


Figure 19. Load Transient (0.5A-4.5A, 1.6A/us)

Figure 20. Load Transient (1.25A-3.75A, 1.6A/us)

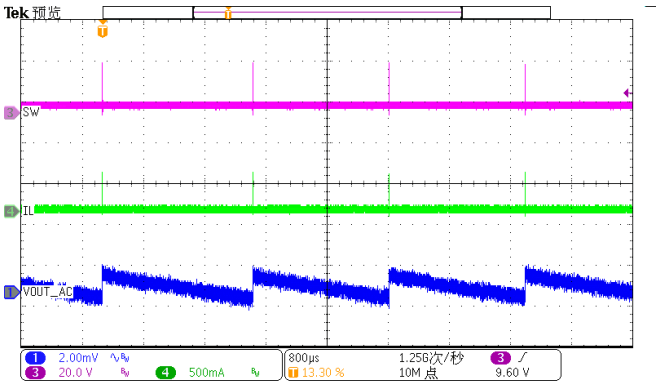


Figure 21. Output Ripple (Iload=0A)

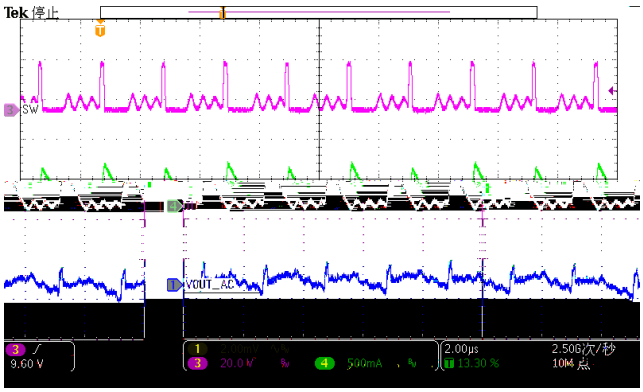


Figure 22. Output Ripple (Iload=100mA)

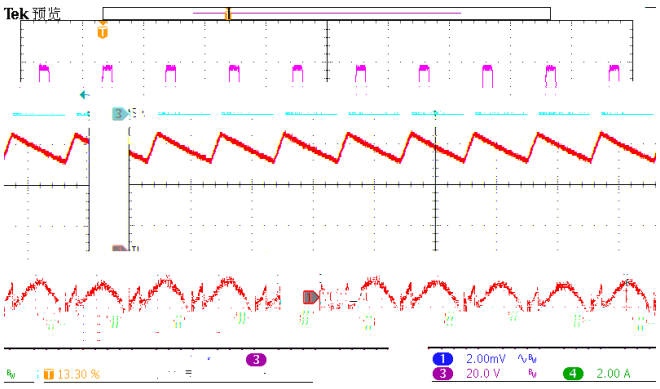


Figure 23. Output Ripple (Iload=5A)

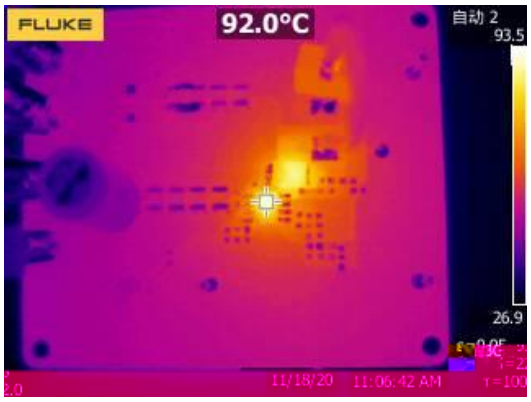


Figure 24. Thermal, 24VIN, 3.3Vout,5A

Proper PCB layout is a critical for SCT2650's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Freewheeling diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
6. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
7. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
8. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
9. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
10. For achieving better thermal performance, a four-layer layout is strongly recommended.

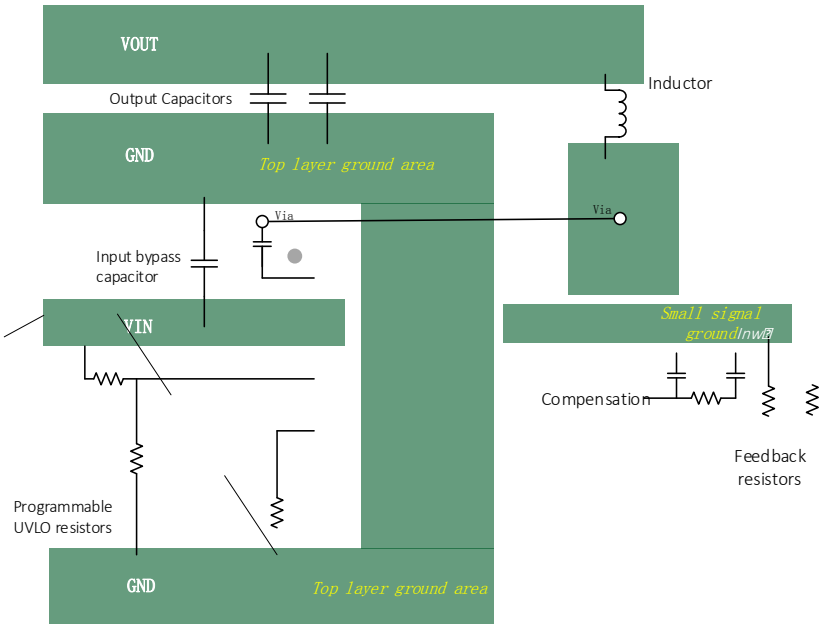
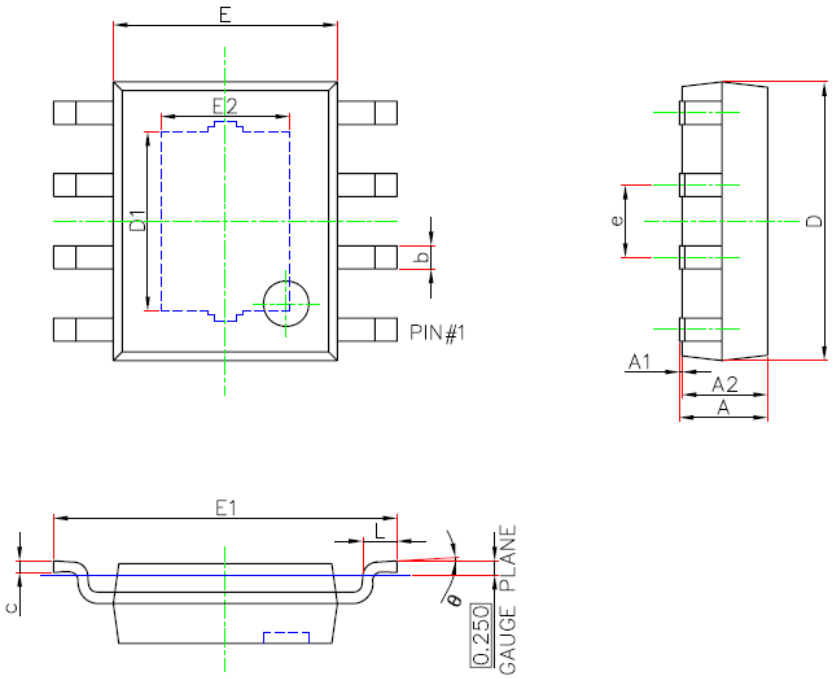


Figure 25. PCB Layout Example



SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

Orderable Device	Package Type	Pins	SPQ
SCT2650STER	ESOP	8	4000