- Wide Input Voltage Range: 2.7V-14.0V
- Wide Output Voltage Range: 4.5V-14.6V
- Fully Integrated High-side/Low-side Power MOSFETs：13m /11m
- Up to 12A Switch Current and Programmable Peak Current LimitMon
- Typical Shut-down Current: 1uA
- Programmable Switching Frequency: 200kHz-2.2MHz
- Output Overvoltage Protection

FB	17	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference value of 1.2V typical.
COMP	18	Output of the error amplifier and switching converter loop compensation point.
ILIM	19	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.
AGND	20	Analog ground. Analog ground should be used as the common ground for all small signal analog inputs and compensation components. No electrical connection to PGND inside.
PGND	21	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved thermal performance and electrical contact.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	14	V
V_{OUT}	Output voltage range	4.5	14.6	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	DFN-20L	UNIT
R	Junction to ambient thermal resistance (1)	38	°C/W
R	Junction to case thermal resistance (1)	39	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT12A0 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT12A0. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		14	V
V_{OUT}	Output voltage range		4.5V		14.6	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.6 200	2.7	V mV
I_{SD}	Shutdown current	EN=0, No load. Measured on VIN pin		1	3	uA
I_Q	Quiescent current from VIN	EN=2V, No load, No switching. Measured on VIN pin.		1		uA
	Quiescent current from VOUT			120	200	uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.8		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	FPWM mode	1.170	1.202	1.220	V
		PSM mode	1.192	1.210	1.228	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		190		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=1V R_{ILIM}		1.5		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.5V, R_{ILIM} M		0.6		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			13		
R_{DSON_L}	Low side FET on-resistance			11		
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}	10.5	12	13	A
Enable and Mode						
V_{EN}	Enable high threshold Enable low threshold	V_{CC}=5V	 0.4		1.2	V V
R_{EN}	Enable pull down resistance			800		
V_{MODE}	MODE high threshold MODE low threshold	V_{CC}=5V	 1.5		4	V V
R_{MODE}	MODE pull-up resistance			270		
I_{SS}	Soft-start charging current			5		uA
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=301k, V_{OUT}=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=301k, V_{OUT}=12V		150	200	ns
T_{OFF_MIN}	Minimum off-time	R_{FSW}=301k, V_{FB}=0V		100	150	ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold Hysteresis	V_{OUT} rising		15.4 250		V mV
V_{OVP_VFB}	Feedback overvoltage with respect to reference voltage	V_{FB} rising V_{FB} falling		110 105		% %

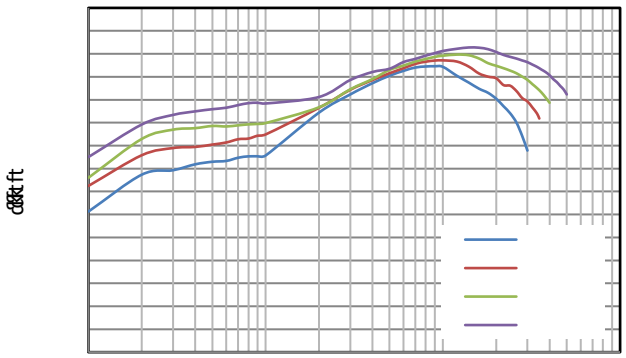


Figure 1. Efficiency, Vout=9V, fsw=560KHz, PFM

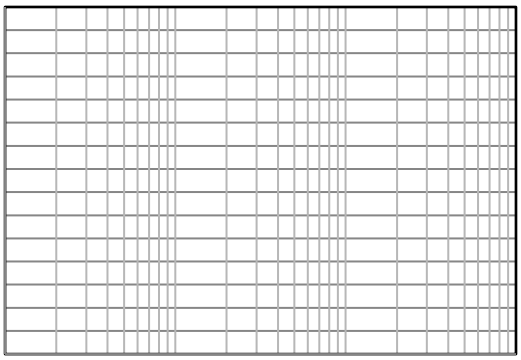


Figure 2. Efficiency, Vin=3.6V, fsw=560KHz, PFM

Figure 3. Efficiency, Vout=9V, fsw=560KHz, PWM

Figure 4. Efficiency, Vin=3.6V, fsw=560KHz, PWM

Figure 5. Switching Frequency vs FSW Resistance

Figure 6. Inductor Peak Current Limit vs RLIM Resistance

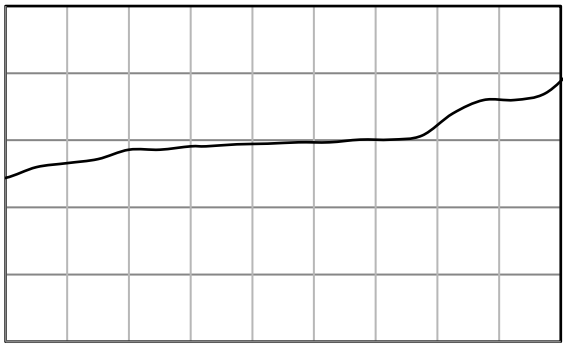


Figure 7. Frequency vs Temperature

Figure 8. Quiescent Current vs Temperature

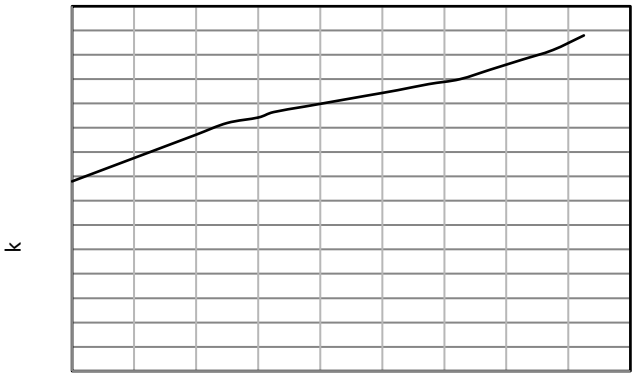


Figure 9. Shutdown Current vs Temperature

Figure 10. Feedback Reference Voltage vs Temperature

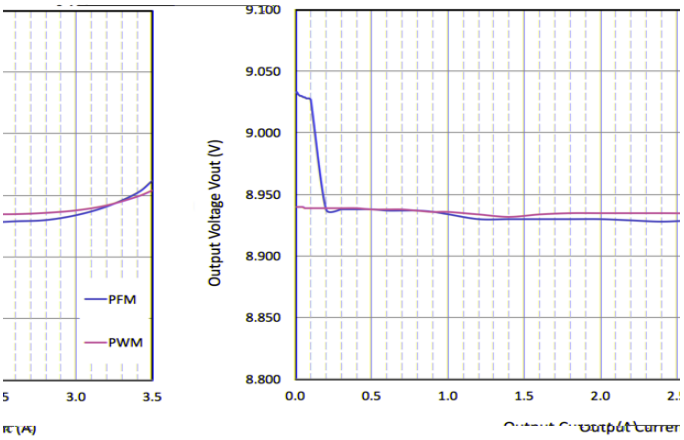


Figure 11. Load Regulation (Vin=3.6V, Vout=9V)

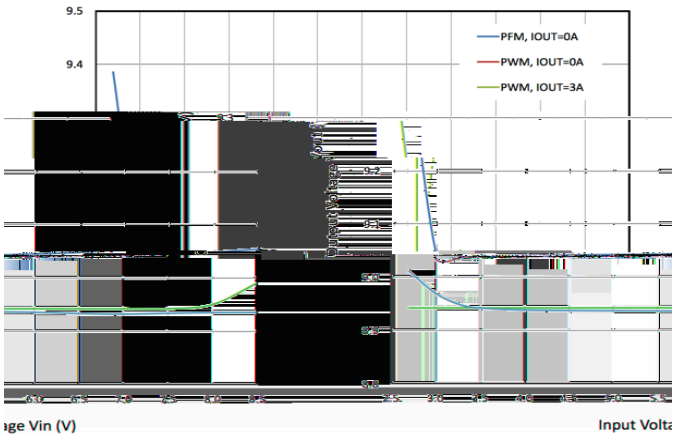
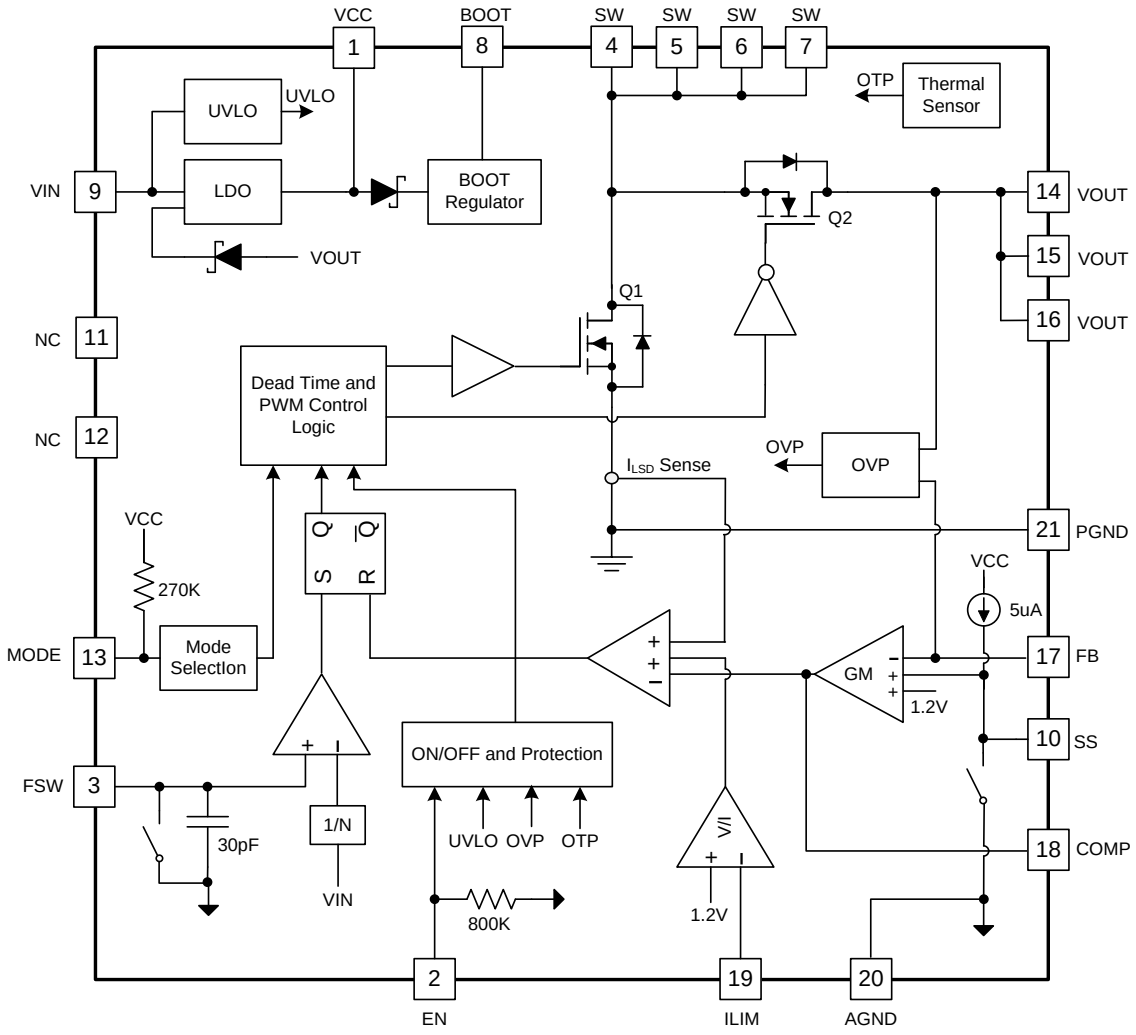


Figure 12. Line Regulation



Overview

The SCT12A0 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control

Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT12A0 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold (minimum 0.4V). the ground. Floating EN pin automatically disables the device.

The SCT12A0 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 5 current charging an external soft-start capacitor C_{SS} when EN pin exceeds turn-on threshold. The device uses the lower voltage between the internal voltage reference 1.2V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1.2V reference. Use equation 1 to calculate the soft-start time (10% to 90%). When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

(1)

where

- t_{SS} is the soft start time
- V_{REF} is the internal reference voltage of 1.2V
- C_{SS} is the capacitance connecting to SS pin
- I_{SS} is the source current of 5uA to SS pin

Adjustable Switching Frequency

The SCT612A0 features adjustable switching frequency from 200kHz to 2.2MHz. To set the switching frequency, an external resistor between SW pin and FSW pin is a must to guarantee the proper operation. Use Equation 2 or the curves in Figure 5 to determine the resistance for a given switching frequency. To reduce the solution size, one would typically set the switching frequency as higher as possible, but need to consider the tradeoff of the thermal dissipation and minimum on time of low-side power MOSFET.

(2)

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Adjustable Peak Current Limit

The SCT12A0 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during over current condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 3 or Figure 6 to calculate the peak current limit.

(3)

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Once VIN is present, VOUT is moved to VIN level due to the direct path from input to output even when the device is shut down or the load is not ready. The presence of unwanted output voltage before system start up sequence could cause system latch off or malfunction.

To address the above issue, users need design external circuits for protection or choose SCT12A1 from Silicon Content Technology, which provides an option to insert an external P-channel MOSFET to disconnect output from input in application. Refer SCT12A1 data sheet for details of load disconnection feature.

Over Voltage Protection and Minimum On-time

The SCT12A0 features both VOUT pin over voltage protection and the FB pin over voltage protection. If the VOUT pin is above 15.4V typical or FB pin voltage exceeds 1.32V typical, the device stops switching immediately until the VOUT pin drops below 15.2 V or FB pin voltage drops below 1.26V. The OVP function prevents the connected output circuitry from un-predictive overvoltage. Featured feedback overvoltage protection prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The low-side MOSFET has minimum on-time 150ns typical limitation. While the device is operating at minimum on time and further increasing Vin pushed output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Forced PWM and PFM Modes

Connecting MODE pin to ground, the SCT12A0 forces the device operating at forced Pulse Width Modulation (PWM) mode with pseudo-fixed switching frequency regardless loading current. Operating in PWM mode can avoid the possible audible noise caused by lower frequency in PFM mode at light load. When the load current approaches zero, the high-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Floating MODE pin or connecting MODE pin to VCC, the SCT12A0 works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the load current decreasing, the COMP pin voltage decreases as resulting the inductor current down. With the load current further decreasing, the COMP pin voltage decreases and be clamped to a voltage corresponding to the ILIM/12. The converter extends the off time of high-side MOSFET Q2 to reduce the average delivered current to output. The switching frequency is lower and varied depending on loading condition. In PFM mode, the peak inductor current is fixed at around 1A and the output voltage is regulated 0.7% higher than the setting output voltage. When the inductor current decreased to zero, zero-cross detection circuitry on high-side MOSFET Q2 forces the Q2 off until the beginning of the next switching cycle. The boost converter does not sink current from the load at light load.

Thermal Shutdown

Once the junction temperature in the SCT12A0 exceeds 150^{O}C, the thermal sensing circuit stops switching until the junction temperature falling below 130C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

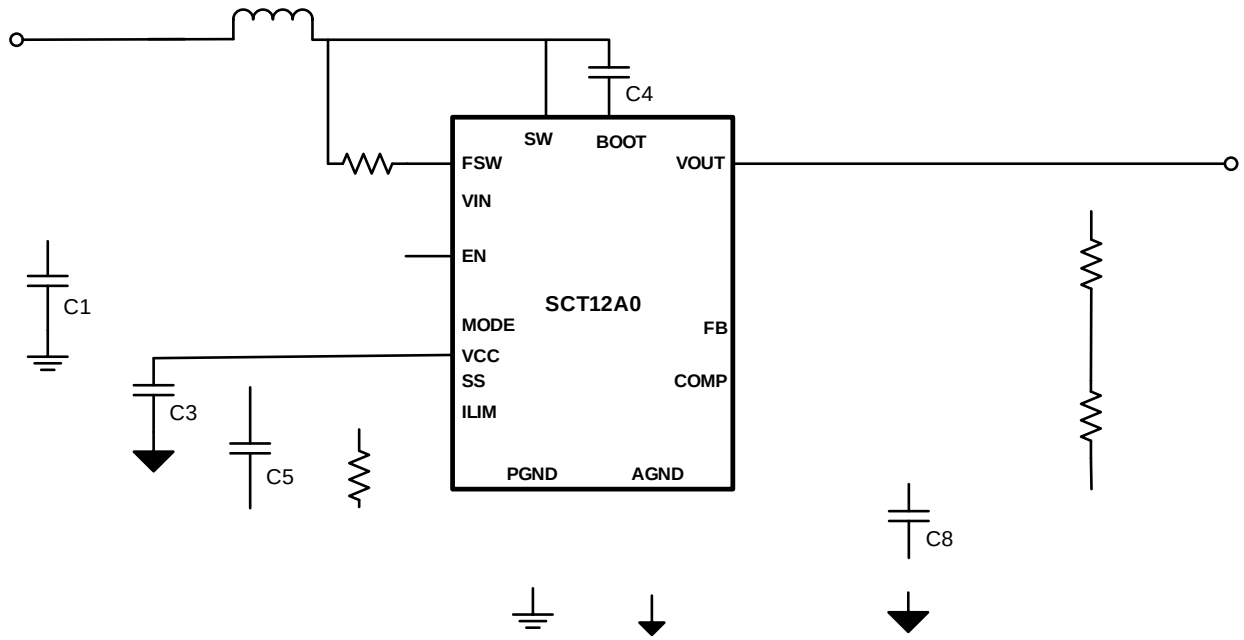


Figure 13. One Cell Battery Input, 9V/3A (30W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.2V
Output Voltage	9V
Output Current	3A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	560 kHz
Operation Mode	PFM

Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 2. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=9V, Room Temperature)

Fsw	R_{FSW}
200 KHz	750
350 KHz	
520 KHz	270
730 KHz	
1000 KHz	127
2000 KHz	

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value fo

Inductor Selection

The performance of
and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency

(10)

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE}

(11)

where

- C_O is the output capacitance

(12)

where

- ESR is the equivalent series resistance of the output capacitor.

(13)

The COMP pin is the output of the internal trans-conductance amplifier. Equation 14 shows the small signal transfer function of compensation network.

(14)

where

- G_{EA} -conductance
- R_{EA}
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- $_{COMP1}$ $_{COMP2}$ are the poles' frequency of the compensation network.
- $_{COMZ}$ is the zero's frequency of the compensation network.

$_{C}$. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/1 $_{SW}$ $_{RHPZ}$.

Then set the value of R5, C8, and C9 in typical application circuit by following these equations.

(15)

where

- $_{C}$ is the selected crossover frequency.

(16)

(17)

If the calculated value of C9 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

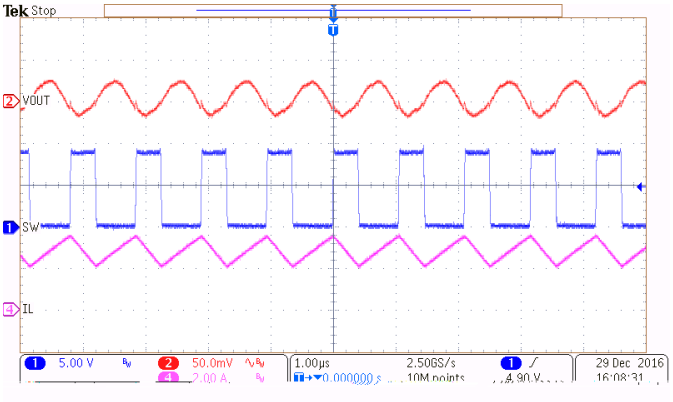


Figure 14. Switching Waveforms and Output Ripple in PWM

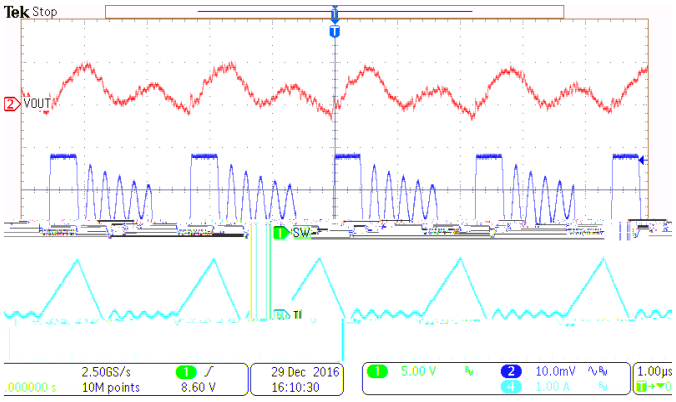


Figure 15. Switching Waveforms and Output Ripple in DCM

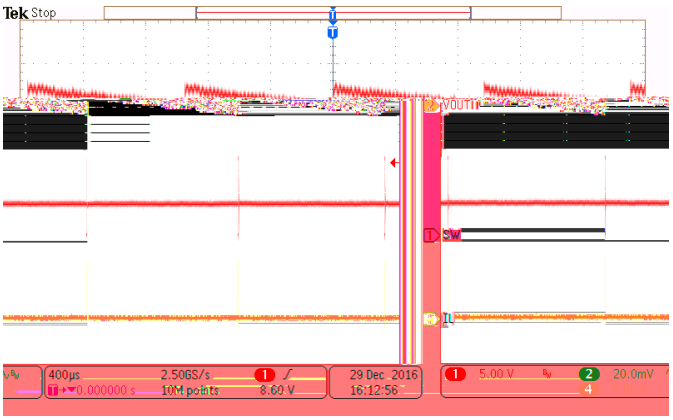


Figure 16. Switching Waveforms in PFM

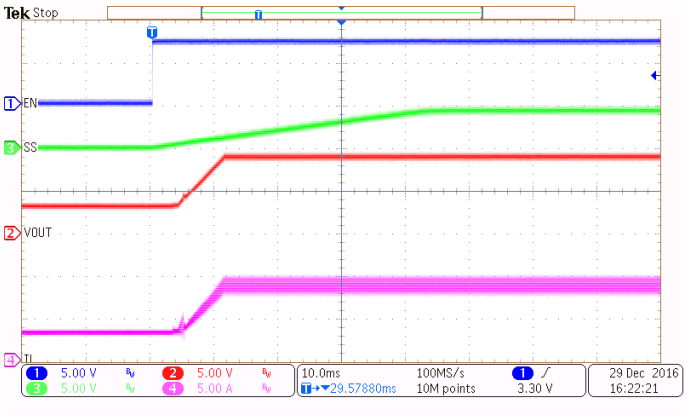


Figure 17. Power Up

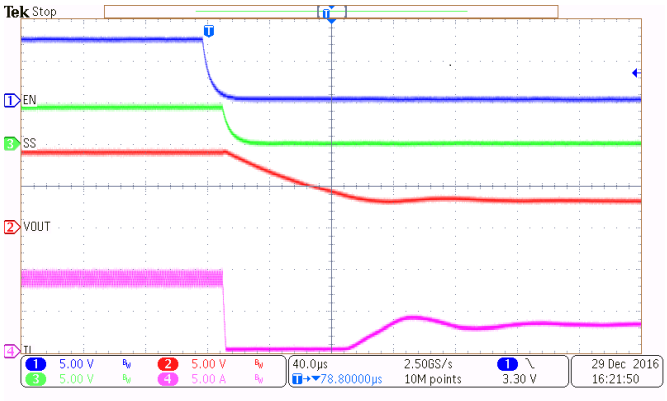


Figure 18. Power Down

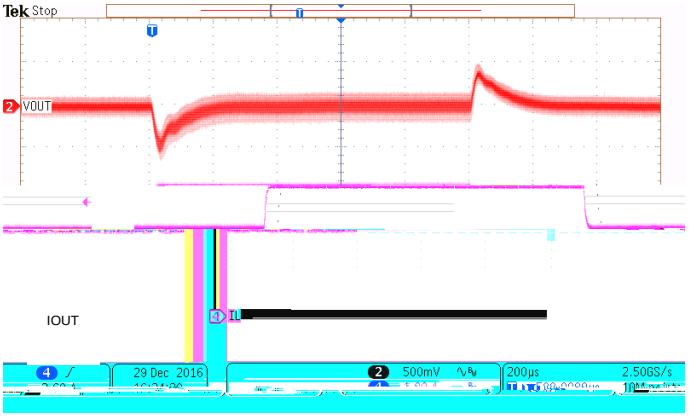


Figure 19. Load Transient (Vout=9V, Iout=2A to 3A, SR=250mA/us)

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and GND pin to reduce the input supply ripple. The placement and ground trace for C6 are critical for the performance of SW ringing voltage. Place capacitor C6 as close to VOUT pin and power ground pad as possible to reduce high frequency ringing voltage on SW pin. Short NC pins to power ground pad directly to reduce the ground trace impedance of C6.

The layout should also be done with well consideration of the thermal. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias under the thermal pad. The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias. Since thermal pad is electrical power ground of the device, improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

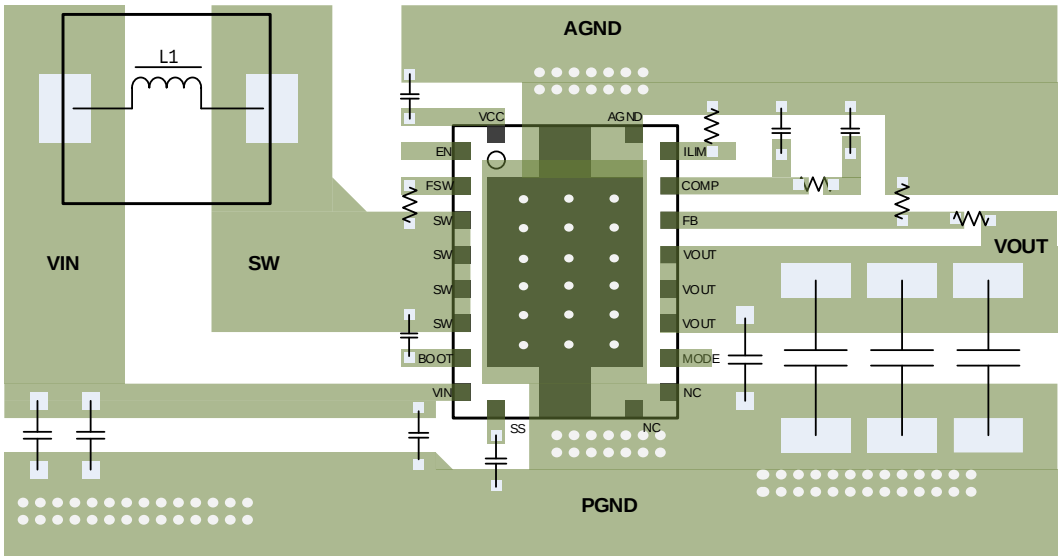


Figure 20. PCB Layout Example Bottom Layer

Thermal Considerations

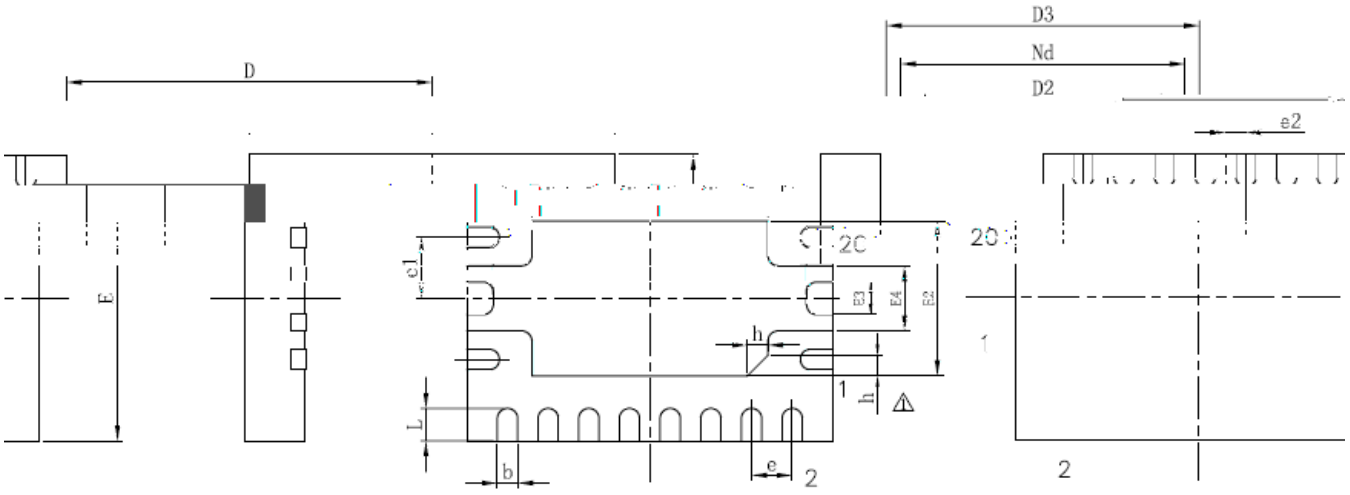
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 18.

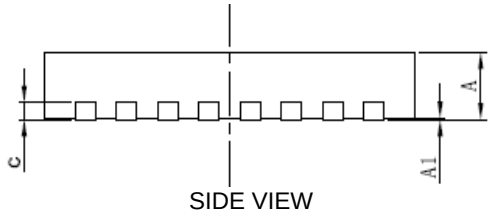
(18)

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT12A0 DFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.



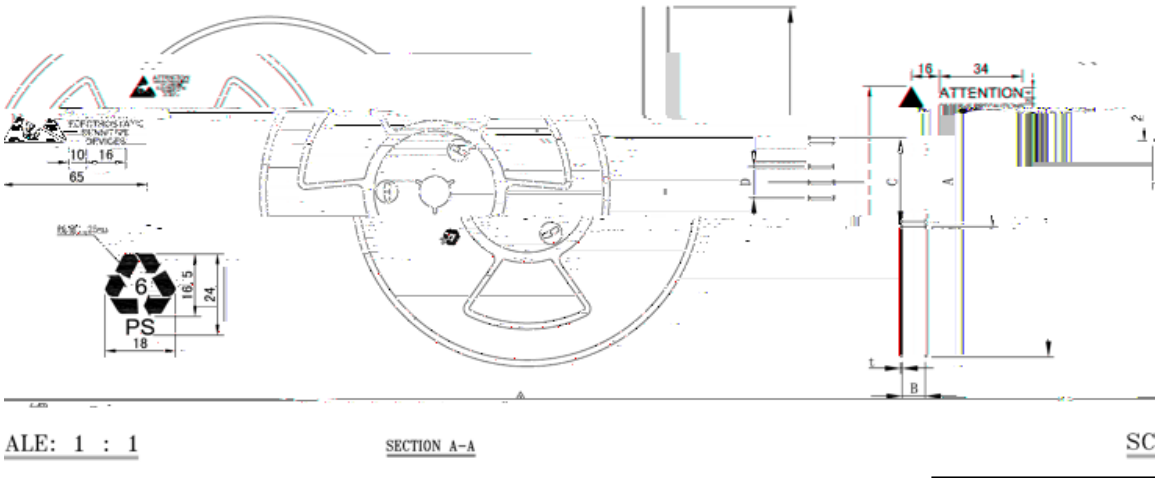


SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.85	0.90	0.95

NOTE:

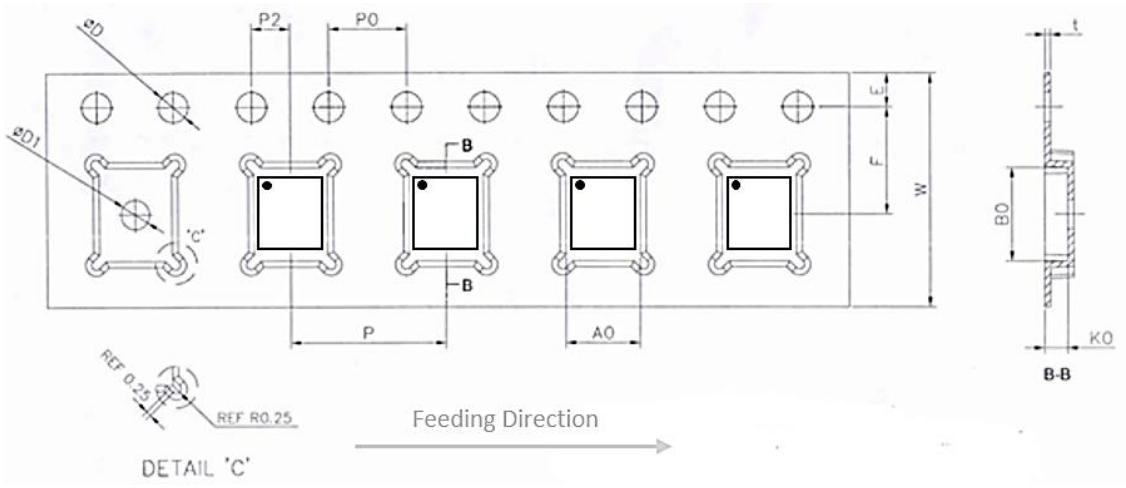
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

Orderable Device	Package Type	Pins	SPQ
SCT12A0DHKR	DFN 3.5mmx4.5mm	20	3000



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3

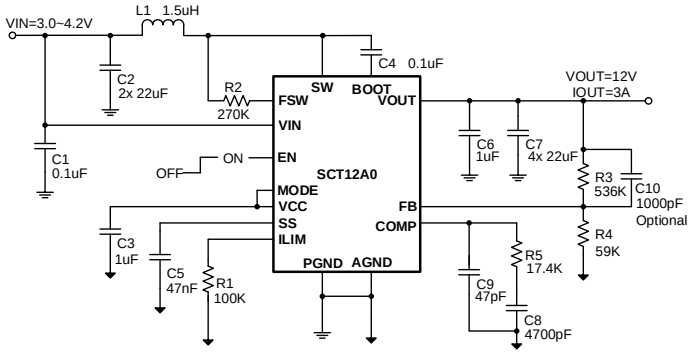


TAPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12±0.30	3.80±0.10	4.80±0.10	1.18±0.10	0.30±0.05	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.10	2.00±0.10	1.55±0.10	1.50MIN	4.00±0.10	40.0±0.20

12V Output, Synchronous Boost Converter



Efficiency, Vin=3.6V

PART NUMBERS	DESCRIPTION	COMMENTS
SCT12A1	30W Fully-integrated Synchronous Boost Converter with Load Disconnection	Vin=2.7V-14V, 12A switch current Load disconnection control to an external PMOS with high-side current sensing to protect • Damage of circuit components and cause catastrophic failure.83 Tl520 0 1 473 334.87 441.5

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