- Wide Input Voltage Range: 2.7V-14.0V
- Wide Output Voltage Range: 4.5V-14.6V
- Fully Integrated 13mΩ High Side FET and 11mΩ Low Side FET
- Up to 92% Efficiency at Vin=3.6V, Vout=9V, and Iout=3A
- Up to 12A Switch Current and Programmable Peak Current Limit
- Load Disconnection Control with an External P-Channel MOSFET
- Typical Shut-down Current: 1uA
- Programmable Switching Frequency: 200kHz-2.2MHz
- Selectable PFM or Forced PWM Mode
- Programmable Soft Start
- Output and Feedback Overvoltage Protection
- Thermal Shutdown Protection: 150°C
- Available in DFN-20 3.5mmx4.5mm Package

- Bluetooth Audio
- Power Banks
- POS System
- E-Cigarette
- USB Power Delivery

The SCT12A1 is a high efficiency synchronous boost converter with fully integrated a 13mΩ high-side MOSFET and an 11mΩ low-side MOSFET, supporting 2.7V to 14V input voltage range and up to 12-A switch current. The switch current limit can be adjustable with an external resistor.

The SCT12A1 adapts constant off-time peak current control to provide fast transient. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions. Using MODE pin selects either Pulse Frequency Modulation (PFM) operation or f

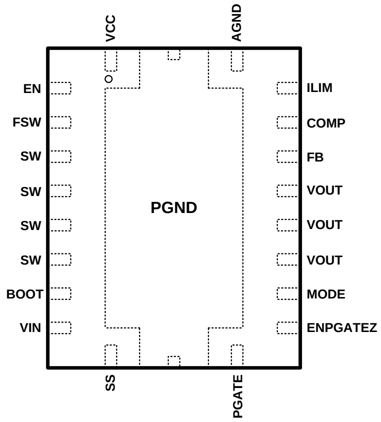
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT12A1	12A1	20-Lead 3.5mm×4.5mm Plastic DFN

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	23.5	V
VIN, SW, VOUT, FSW, PGATE	-0.3	18	V
VCC, LIM FB EN,SS,			

Top View: 20-Lead Plastic DFN 3.5mmx4.5mm



ENPGATEZ	12	Connect the pin to ground to enable the load disconnection control. Directly short to thermal pad under IC to reduce the C6 ground loop if grounding. 400KΩ internal resistor connects this pin to VCC. Floating disables the load disconnection protection.
MODE	13	Operation mode selection. 270KΩ internal resistor connects this pin to VCC. Floating or Logic high enables PFM mode. Logic low enables forced PWM mode.
VOUT	14,15,16	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ringing voltage of SW.
FB	17	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference value of 1.2V typical.
COMP	18	Output of the error amplifier and switching converter loop compensation point.
ILIM	19	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.
AGND	20	Analog ground. Analog ground should be used as the common ground for all small signal analog inputs and compensation components. No electrical connection to PGND inside.
PGND	21	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved thermal performance and electrical contact.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	14	V
V_{OUT}	Output voltage range	4.5	14.6	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	DFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	38	°C/W
$R_{\theta JC}$	Junction to case thermal resistance (1)	39	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT12A1 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT12A1. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		14	V
V_{OUT}	Output voltage range		4.5V		14.6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.6	2.7	V
	Hysteresis			200		mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1	3	uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching ENPGATEZ=floating		1		uA
	Quiescent current from VOUT			120	200	uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.8		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	FPWM mode	1.170	1.202	1.220	V
		PSM mode	1.192	1.210	1.228	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		190		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=1V R_{ILIM}=100KΩ		1.5		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.5V, R_{ILIM}=100KΩ,PFM		0.6		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			13		mΩ
R_{DSON_L}	Low side FET on-resistance			11		mΩ
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100kΩ	10.5	12	13	A
Enable and Mode						
V_{EN}	Enable high threshold	V_{CC}=5V			1.2	V
	Enable low threshold		0.4			V
R_{EN}	Enable pull down resistance			800		kΩ
V_{MODE}	MODE high threshold	V_{CC}=5V			4	V
	MODE low threshold					

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{PGATE}	PGATE pull down current			60		uA
V_{PGATE_C}	Clamp voltage between PGATE and VOUT			7.1	8	V
Protection						
V_{OVP_VOUT}	Output overvoltage threshold	V_{OUT} rising		15.4		V
	Hysteresis					

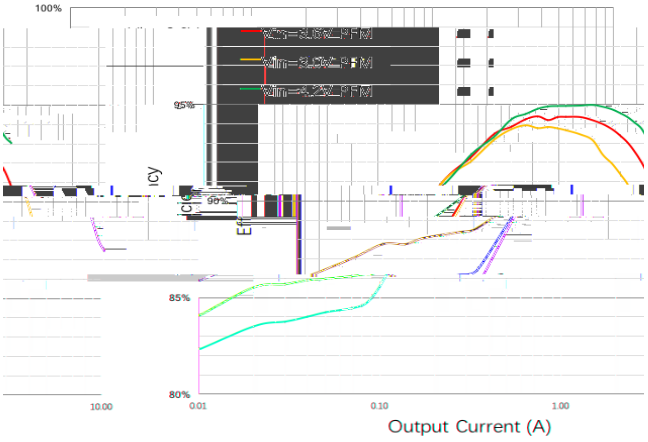


Figure 1. Efficiency, Vout=9V, fsw=560KHz, PFM

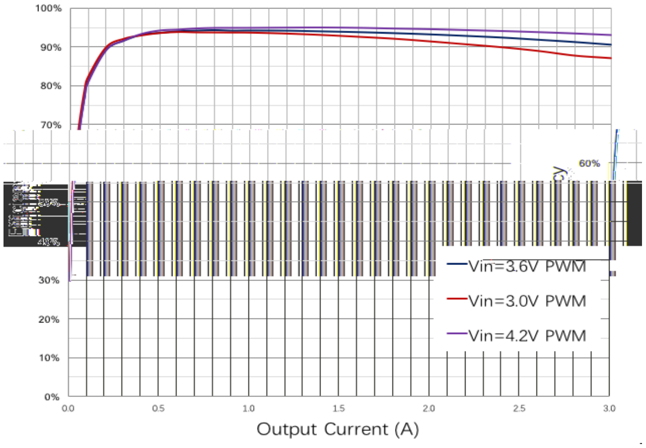


Figure 2. Efficiency, Vout=9V, fsw=560KHz, PWM

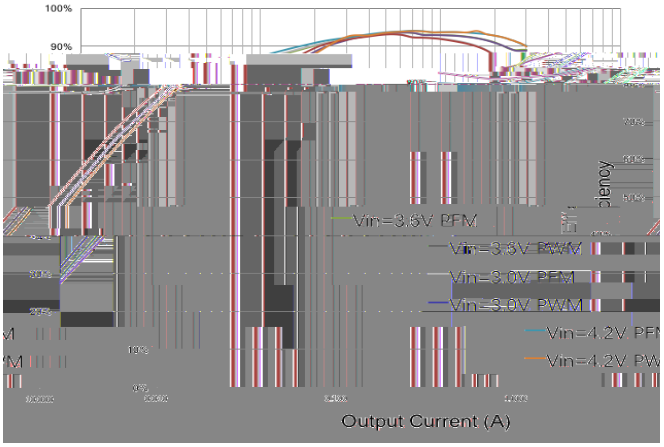


Figure 3. Efficiency, Vout=12V, fsw=560KHz, 1-cell Battery

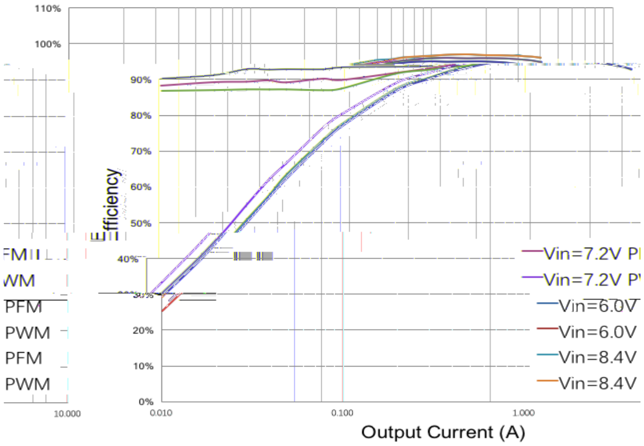


Figure 4. Efficiency, Vout=12V, fsw=560KHz, 2-cells Battery

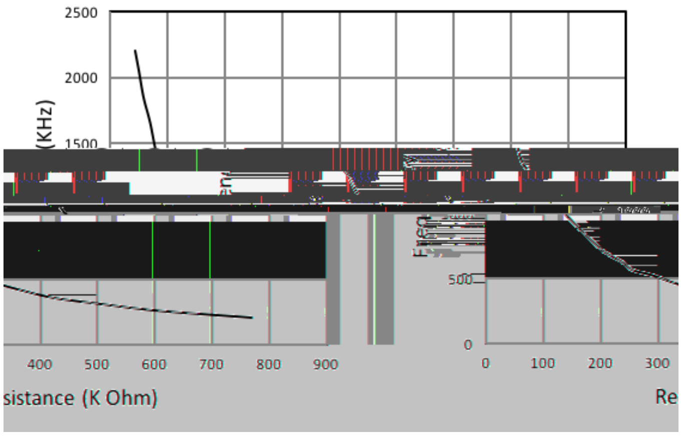


Figure 5. Switching Frequency vs FSW Resistance

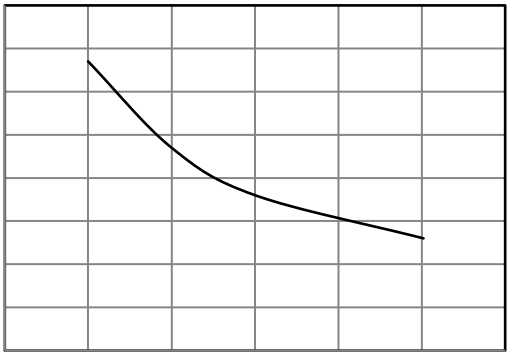


Figure 6. Inductor Peak Current Limit vs RLIM Resistance

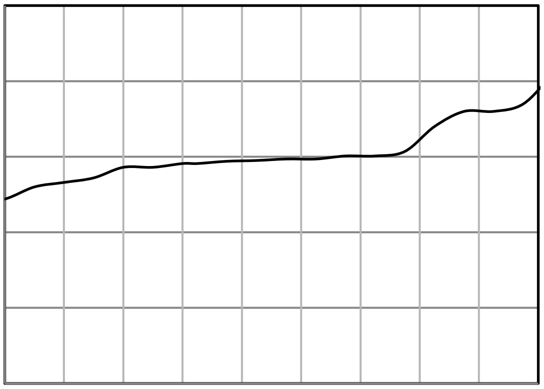


Figure 7. Frequency vs Temperature

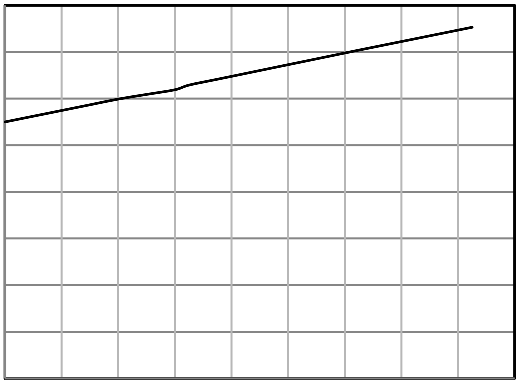


Figure 8. Quiescent Current vs Temperature

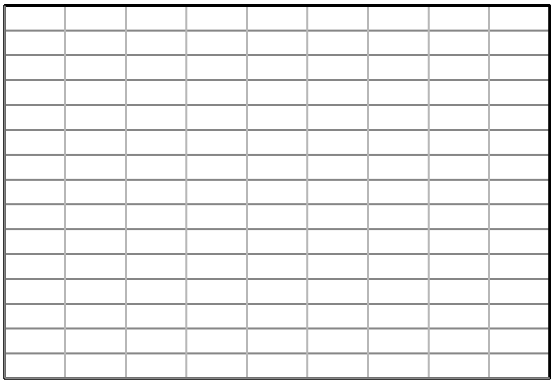
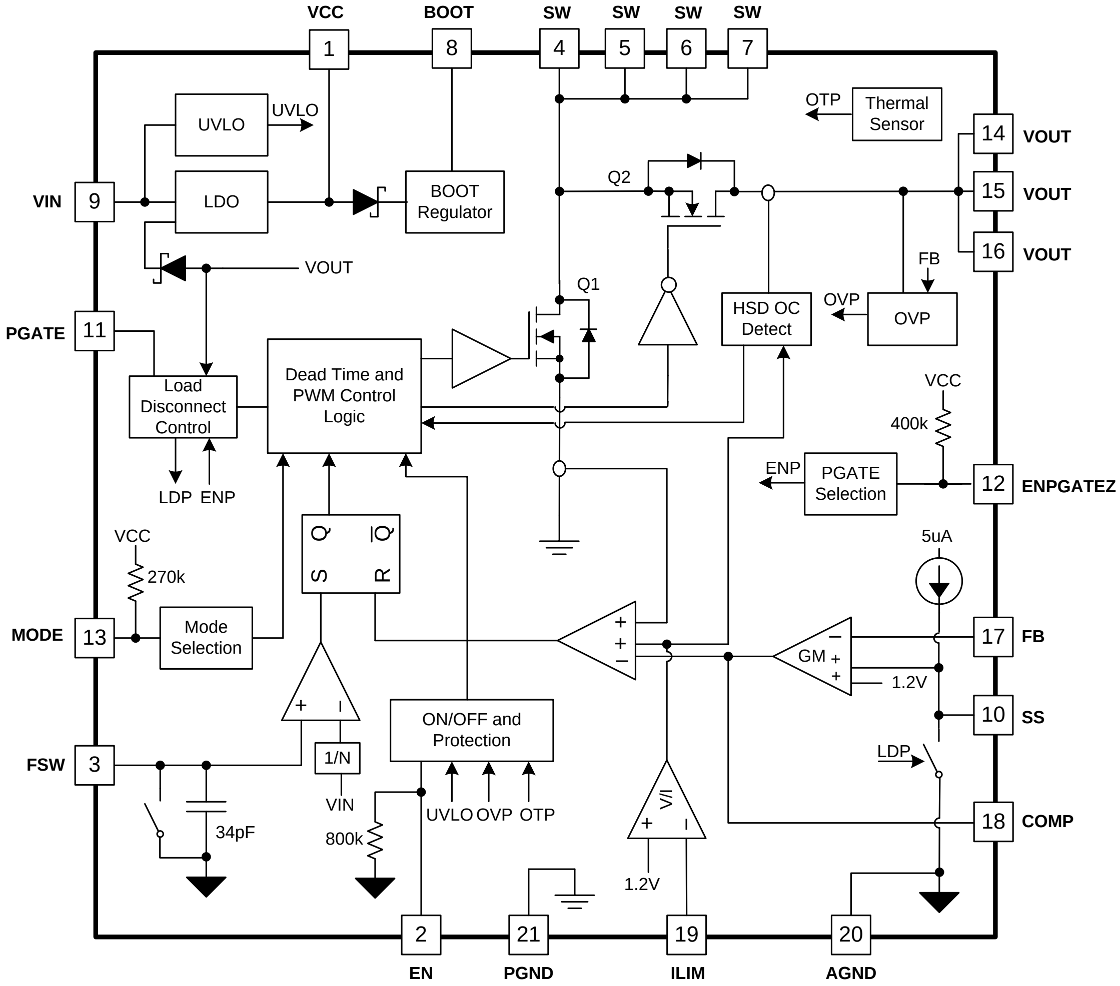


Figure 9. Shutdown Current vs Temperature

Figure 10. Feedback Reference Voltage vs Temperature

Figure 11. Load Regulation (Vin=3.6V, Vout=9V)

Figure 12. Line Regulation


VCC
BOOT
SW
SW
SW
SW
1
8
4
5
6
7
UVLO
UVLO
LDO
VIN
9
BOOT Regulator
Q2
OTP
Thermal Sensor
14
VOUT
15
VOUT
16
VOUT
VOUT
FB
Q1
HSD OC Detect
OVP
OVP
PGATE
11
Load Disconnect Control
Dead Time and PWM Control Logic
VCC
400k
LDP
ENP
ENP
PGATE Selection
12
ENPGATEZ
VCC
270k
Q
Q̄
S
R
5uA
MODE
13
Mode Selection
GM
17
FB
1.2V
10
SS
FSW
3
1/N
ON/OFF and Protection
LDP
18
COMP
34pF
VIN
800k
UVLO
OVP
OTP
1.2V
2
EN
21
PGND
19
ILIM
20
AGND

Overview

The SCT12A1 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage of COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases.

Under Voltage Lockout UVLO

The SCT12A1 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.6V typical at startup and falling threshold is 2.4V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.1V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT12A1 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold (minimum 0.4V). An internal 800KΩ resistor connects EN pin to the ground. Floating EN pin automatically disables the device.

The SCT12A1 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 5μA current charging an external soft-start capacitor C_{SS} when EN pin exceeds turn-on threshold. The device uses the lower voltage between the internal voltage reference 1.2V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1.2V reference. Use equation 1 to calculate the soft-start time (10% to 90%). When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

(1)

where

- t_{SS} is the soft start time
- V_{REF} is the internal reference voltage of 1.2V
- C_{SS} is the capacitance connecting to SS pin
- I_{SS} is the source current of 5uA to SS pin

Adjustable Switching Frequency

The SCT12A1 features adjustable switching frequency from 200kHz to 2.2MHz. To set the switching frequency, an external by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 3 or Figure 6 to calculate the peak current limit.

$$\frac{}{} \tag{3}$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Load Disconnection Control (SCT Patent Filed)

For both non-synchronous and synchronous boost converter, there is a non-fully controlled current path from converter input to output load through the diode or the high-side MOSFET body diode. During start up, once VIN is present, VOUT is moved to VIN level due to the direct path from input to output even when the device is shut down or the load is not ready. The presence of unwanted output voltage before system start up sequence could cause system to latch off or malfunction. When the output shorts to ground at fault condition, the direct path causes the inductor current running away, the converter active components damages, and the catastrophic failure at load circuit.

To address the above issues, the SCT12A1 provides a solution to insert an external P-channel MOSFET to disconnect the load from the converter output in application as shown in Figure 13. Choosing a lower R_{dson} of the disconnection P-channel MOSFET Q3 reduces impact on the efficiency. The source of Q3 needs connect to VOUT pin. Output capacitor is required at both VOUT pin and the source of P-channel MOSFET to maintain the loop stability.

In Figure 13, connecting ENPGATEZ pin to ground enables load disconnection features of SCT12A1. PGATE pin connecting to gate of Q3 has a constant sink current pulling down capability and a resistance pulling up capability. During SCT12A1 starting up, internal circuitry softly starts up of P-channel MOSFET. When gate-source voltage of external P-channel MOSFET is lower than the threshold voltage, the Q3 is turned on and the load is connected to VOUT pin. The source-gate voltage of external P-channel MOSFET is clamped up to 8V when the P-channel MOSFET is fully turned on.

To detect if SCT12A1 has serve over loading or output hard short condition, the SCT12A1 has the current sensing scheme on internal high-side MOSFET during its turn-on state as shown Figure 13. When the high side MOSFET over current is detected, SS pin is discharged to ground and the external P-channel MOSFET is turned off immediately. The load is disconnected from the converter output. When high-side MOSFET is turned off, the SCT12A1 compares the VIN and VOUT, if VOUT is lower than VIN 1V, the SCT12A1 shuts off the external P-channel MOSFET and disconnect the load immediately as well.

If serve over current happens or output shorts to ground, the SCT12A1 minimizes the power dissipation by implementing hiccup mode as shown in Figure 14. For example, when internal high-side MOSFET over current triggers load disconnection protection, SS pin resets and the boost converter stops switching. After SS pin starts charging and reaches 1.2V, boost converter resumes to normal switching and starts to turn on P-channel MOSFET again. The hiccup time can be calculated with external capacitance on SS pin as shown in equation 1. If the fault condition disappears, the SCT12A1 resumes to normal operation automatically.

In extreme application case, starting up SCT12A1 with huge output capacitor C5B and heavy load might cause over current protection. Increasing C5A capacitance accordingly enables startup normally.

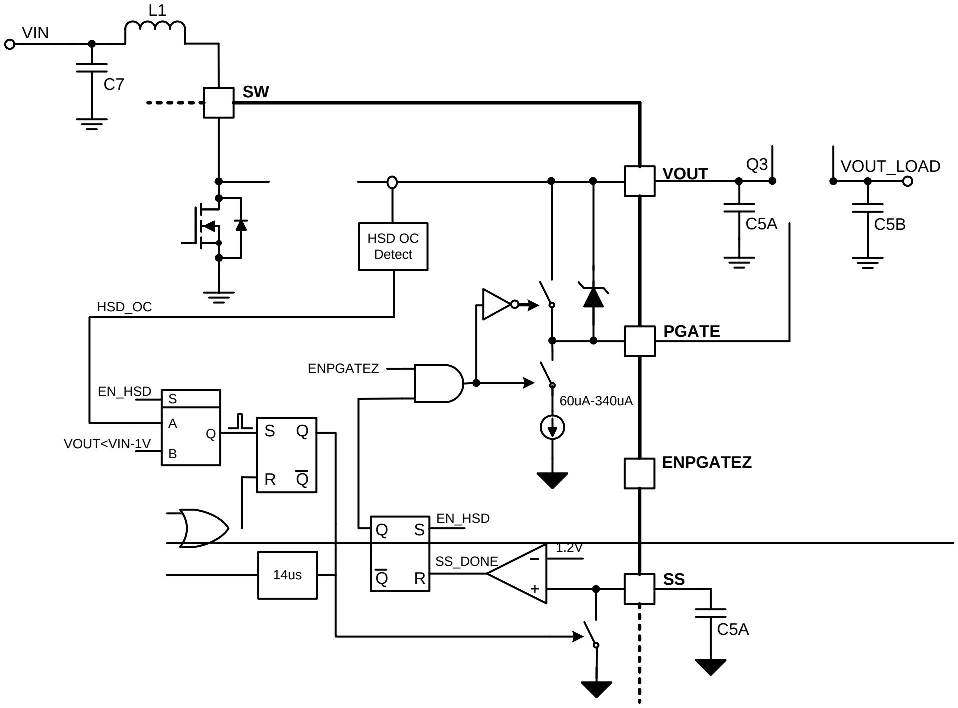


Figure 13. Load Disconnection Control

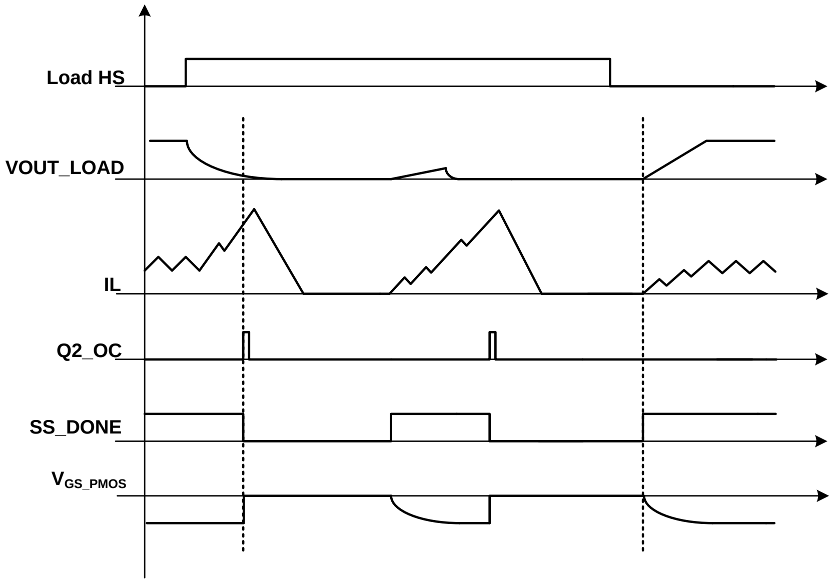


Figure 14. Hiccup Mode Sequence

Over Voltage Protection and Minimum On-time

The SCT12A1 features both VOUT pin over voltage protection and the FB pin over voltage protection. If the VOUT pin is above 15.4V typical or FB pin voltage exceeds 1.32V typical, the device stops switching immediately until the VOUT pin drops below 15.2 V or FB pin voltage drops below 1.26V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

The low-side MOSFET has minimum on-time 150ns typical limitation. While the device is operating at minimum on time and further increasing Vin pushed output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Forced PWM and PFM Modes

Connecting MODE pin to ground, the SCT12A1 forces the device operating at forced Pulse Width Modulation (PWM) mode with pseudo-fixed switching frequency regardless loading current. Operating in PWM mode can avoid the possible audible noise caused by lower frequency in PFM mode at light load. When the load current approaches zero, the high-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Floating MODE pin or connecting MODE pin to VCC, the SCT12A1 works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the load current decreasing, the COMP pin voltage decreases as resulting the inductor current down. With the load current further decreasing, the COMP pin voltage decreases and be clamped to a voltage corresponding to the ILIM/12. The converter extends the off time of high-side MOSFET Q2 to reduce the average delivered current to output. The switching frequency is lower and varied depending on loading condition. In PFM mode, the peak inductor current is fixed at around 1A and the output voltage is regulated 0.7% higher than the setting output voltage. When the inductor current decreased to zero, zero-cross detection circuitry on high-side MOSFET Q2 forces the Q2 off until the beginning of the next switching cycle. The boost converter does not sink current from the load at light load.

Thermal Shutdown

Once the junction temperature in the SCT12A1 exceeds 150C, the thermal sensing circuit stops switching until the junction temperature falling below 130C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

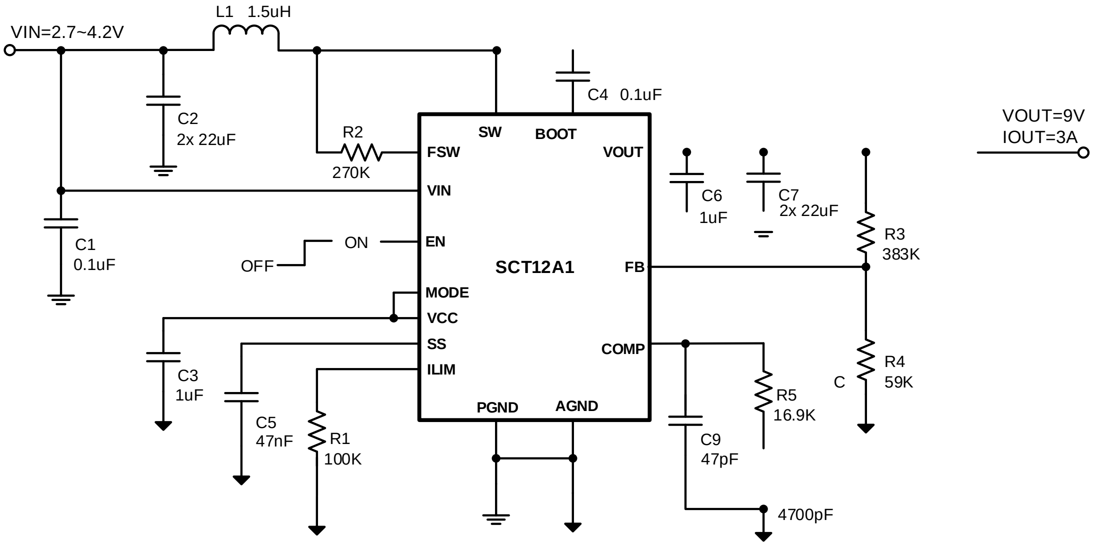


Figure 15. One Cell Battery Input, 9V/3A (30W) Output with Load Disconnection Protection

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 8.4V
Output Voltage	9V
Output Current	3A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	560 kHz
Operation Mode	PFM

For description in the typical application section, the converter output before PMOS is specified as VOUT_P and the converter output after PMOS is specified as VOUT in below.

Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 2. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=9V, Room Temperature)

Fsw	R_{FSW}
200 KHz	750 KΩ
350 KHz	422 KΩ
520 KHz	270 KΩ
730 KHz	196 KΩ
1000 KHz	127 KΩ
2000 KHz	48.7 KΩ

Peak Current Limit

Using equation 3 the correct external resistor at ILIM pin sets the peak input current. For a typical current limit of 12A, the resistor value is 100KΩ. The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Table 2. R_{LIM} Value for Inductor Peak Current (Vin=3.6V, Vout=9V, L=1.5uH, Room Temperature)

I_{LIM}	R_{LIM}
12 A	100 KΩ
8 A	154 KΩ
6.3A	200 KΩ
4.4A	301 KΩ

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 4.

(4)

where:

- V_{REF} is the feedback reference voltage, typical 1.2V

Table 3. Feedback Resistor R_3 R_4Value for Output Voltage (Room Temperature)

V_{OUT}	R_3	R_4
5 V	187 KΩ	59 KΩ
9 V	383 KΩ	59 KΩ
12 V	536 KΩ	59 KΩ

Inductor Selection

The performance of inductor affects the power supply’s steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance values reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as in equation 5

(5)

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 6 user's target application with the previous calculations and bench evaluation. In this application, the WB's inductor CDMC8D28NP-1R2MC is used on SCT12A1 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
WE-HCI SMD 7443552150	1.5	5.3	17 / 14	10.5 x 10.2 x 4.0	WurthElektronix
CDMC8D28NP-1R2MC	1.2	7.0	12.2 / 12.	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT12A1. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasatic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22μF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 8 and 9 to calculate the minimu4(c)-5(ti)6(v)-5(e 0000 0 1 252.89 407.35 Tm0 G[-)]TJETQq0.00000912 0 612 792 reW*nB re1(qeW2 re

VOUT pin voltage in the application. As a result, the low R_{dson} and low threshold P-channel MOSFET is preferred. Table 5 shows the recommended P-channel MOSFET details.

Table 5. Recommended External P-channel MOSFET

Part Number ±	R_{dson} (m)	I_D (A)	Max V_{DS} (V)	Max V_{GS} (V)	Vendor
FDMC612PZ	8.4	14	-20	±12	Fairchild
CSD25404Q3	5.5	18	-20	±12	Texas Instruments

Loop Stability

An external loop compensation network comprises resi

Vend3632.832

Vend3632.8W6re3.21f12/4

5.5QW6re3.25 8 <</4 n/F3

)

The next step is to choose the loop crossover frequency, f_C . The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW} , or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R5, C8, and C9 in typical application circuit by following these equations.

(15)

where

- f_C is the selected crossover frequency.

(16)

(17)

If the calculated value of C9 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Test Condition: VIN=3.6V, VOUT=9V, T_a=27 C.

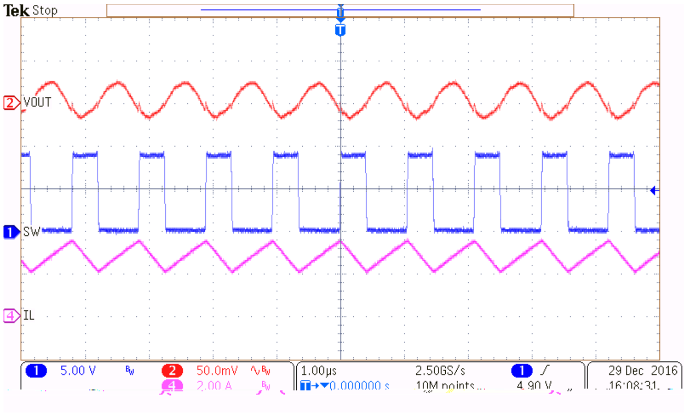


Figure 16. Switching Waveforms and Output Ripple in PWM

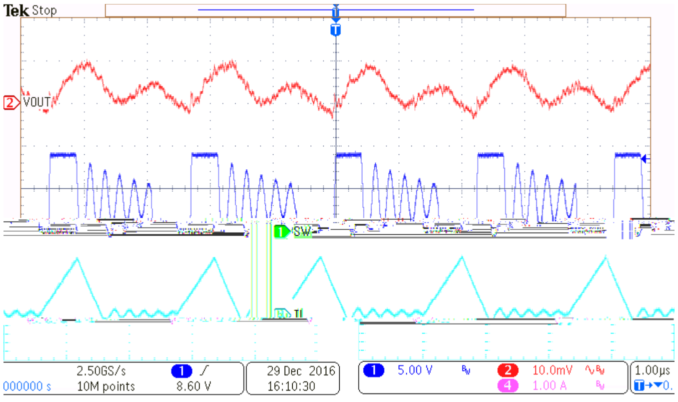


Figure 17. Switching Waveforms and Output Ripple in DCM

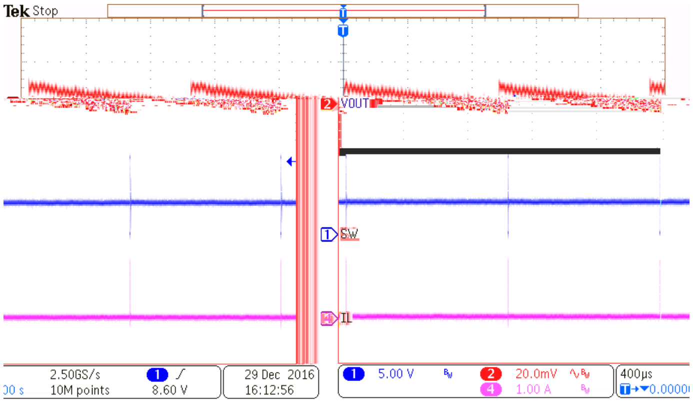


Figure 18. Switching Waveforms in PFM

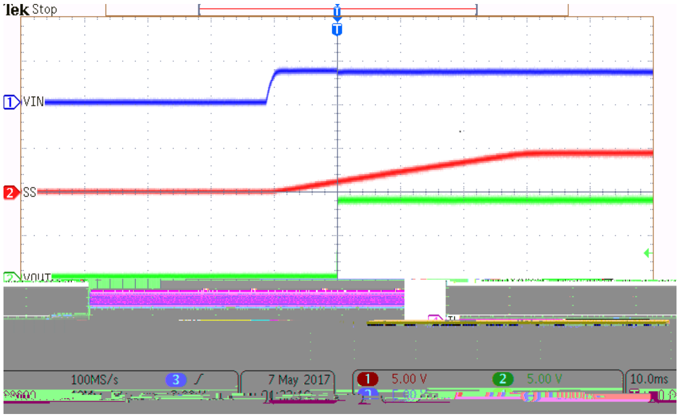


Figure 19. Power Up

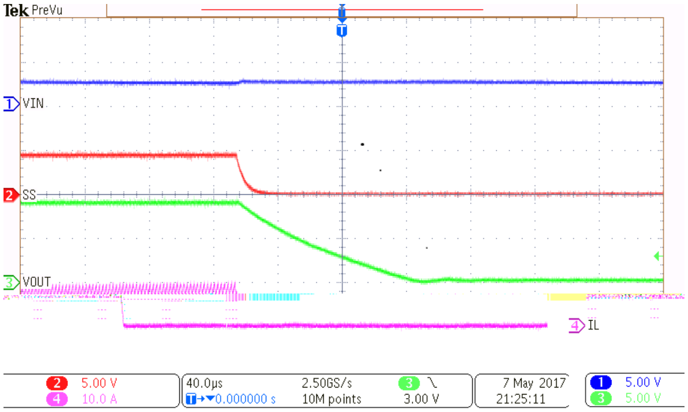


Figure 20. Power Down

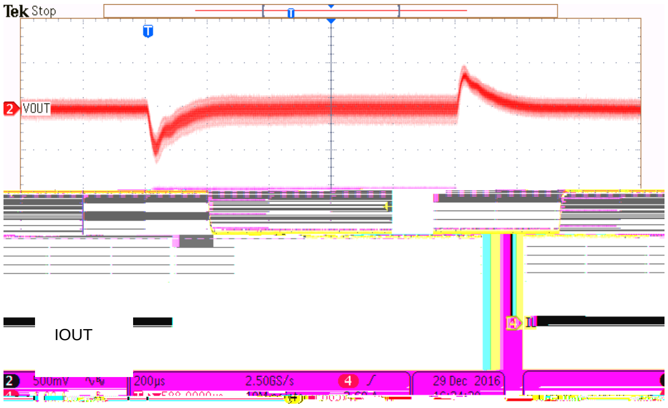


Figure 21. Load Transient
(Vout=9V, Iout=2A to 3A, SR=250mA/us)

Figure 22. PSM, Output Hard Short with 0A Load

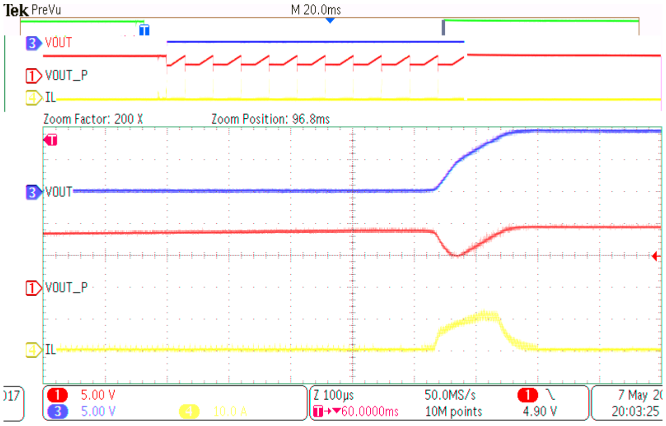


Figure 23. PSM, Output Hard Short Recovery

Figure 24. Output Hard Short with 3A Load

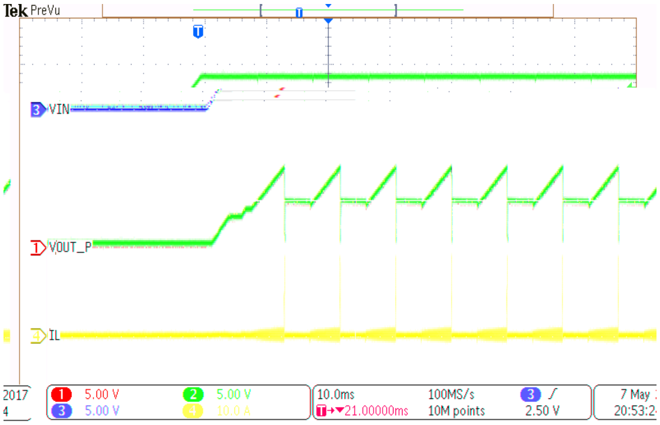


Figure 25. Soft Start with Output Hard Short

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple. The placement and ground trace for C6 is critical for the performance of SW ringing voltage. Place capacitor C6 as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin. Connect ENPGATEZ pin to power ground pad under IC to reduce the ground trace impedance of C6, if ENPGATEZ grounding.

The layout should also be done with well consideration of the thermal. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias. Since thermal pad is electrical power ground of the device, improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

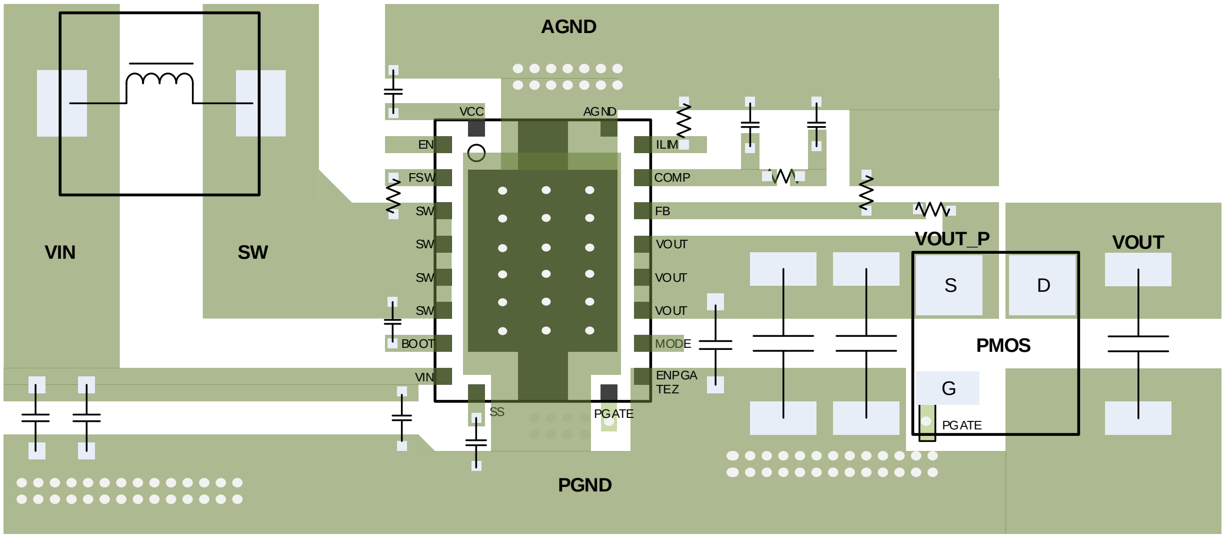


Figure 26. PCB Layout Example Top Layer

Thermal Considerations

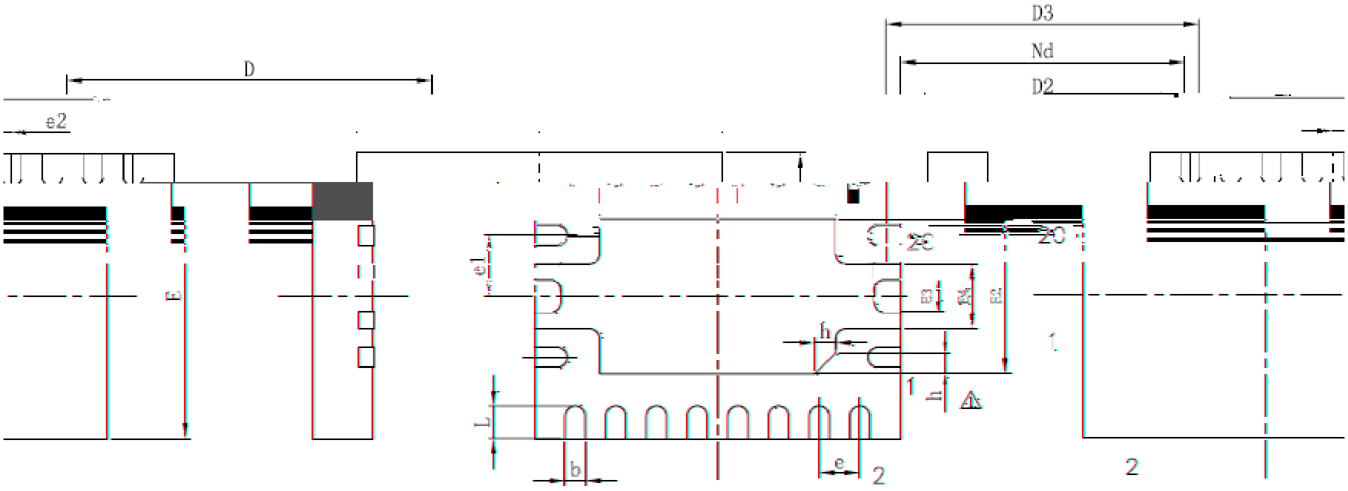
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 18.

(18)

where

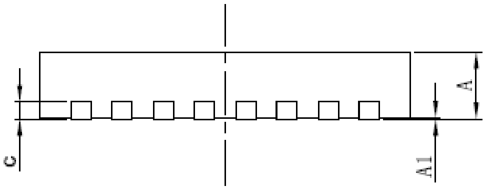
- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT12A1 DFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.



TOP VIEW

BOTTOM VIEW



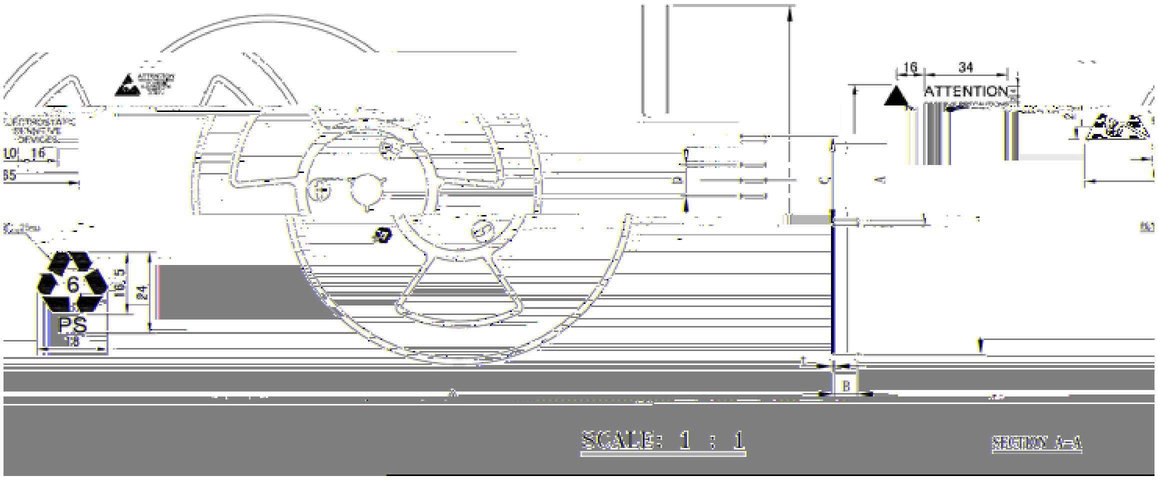
SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

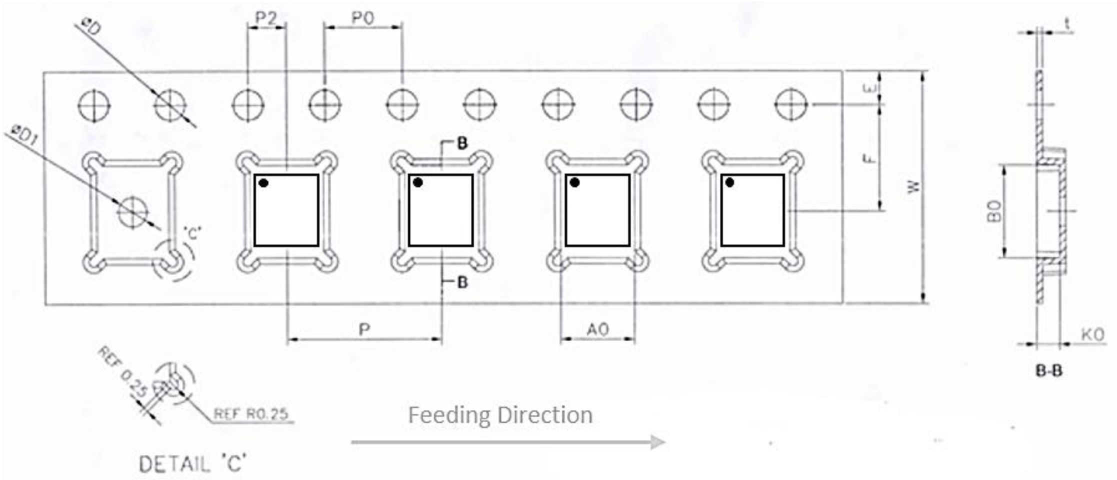
SYMBOL	**Unit: Millimeter**		
	MIN	**TYP**	**MAX**
A	0.85	0.9	0.95
A1	——	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.40	4.50	4.60
D2	3.10	3.20	3.30
D3	3.85REF		
e	0.50BSC		
e1	0.75BSC		
e2	0.25BSC		
Nd	3.50BSC		
E	3.40	3.50	3.60
E2	2.10	2.20	2.30
E3	0.35REF		
E4	0.75REF		
L	0.35	0.40	0.45
h	0.20	0.25	0.30

Device	Package Type	Pins	SPQ
SCT12A1DHKR	DFN	20	3000



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TYPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12±0.30	3.80±0.10	4.80±0.10	1.18±0.10	0.30±0.05	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.10	2.00±0.10	1.55±0.10	1.50MIN	4.00±0.10	40.0±0.20

PART NUMBERS	DESCRIPTION	COMMENTS
SCT12A0	10-A Fully-integrated Synchronous Boost Converter	Vin=2.7V-14V, 12A switch peak current No load disconnection control

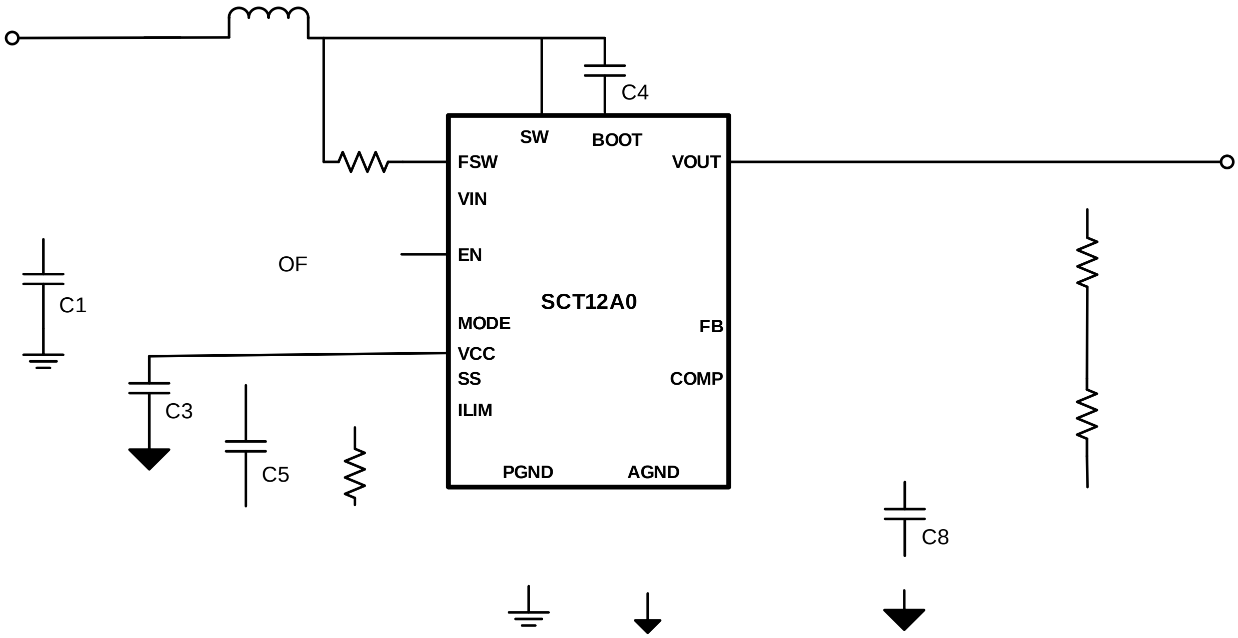


Figure 27. SCT12A0 Typical Application