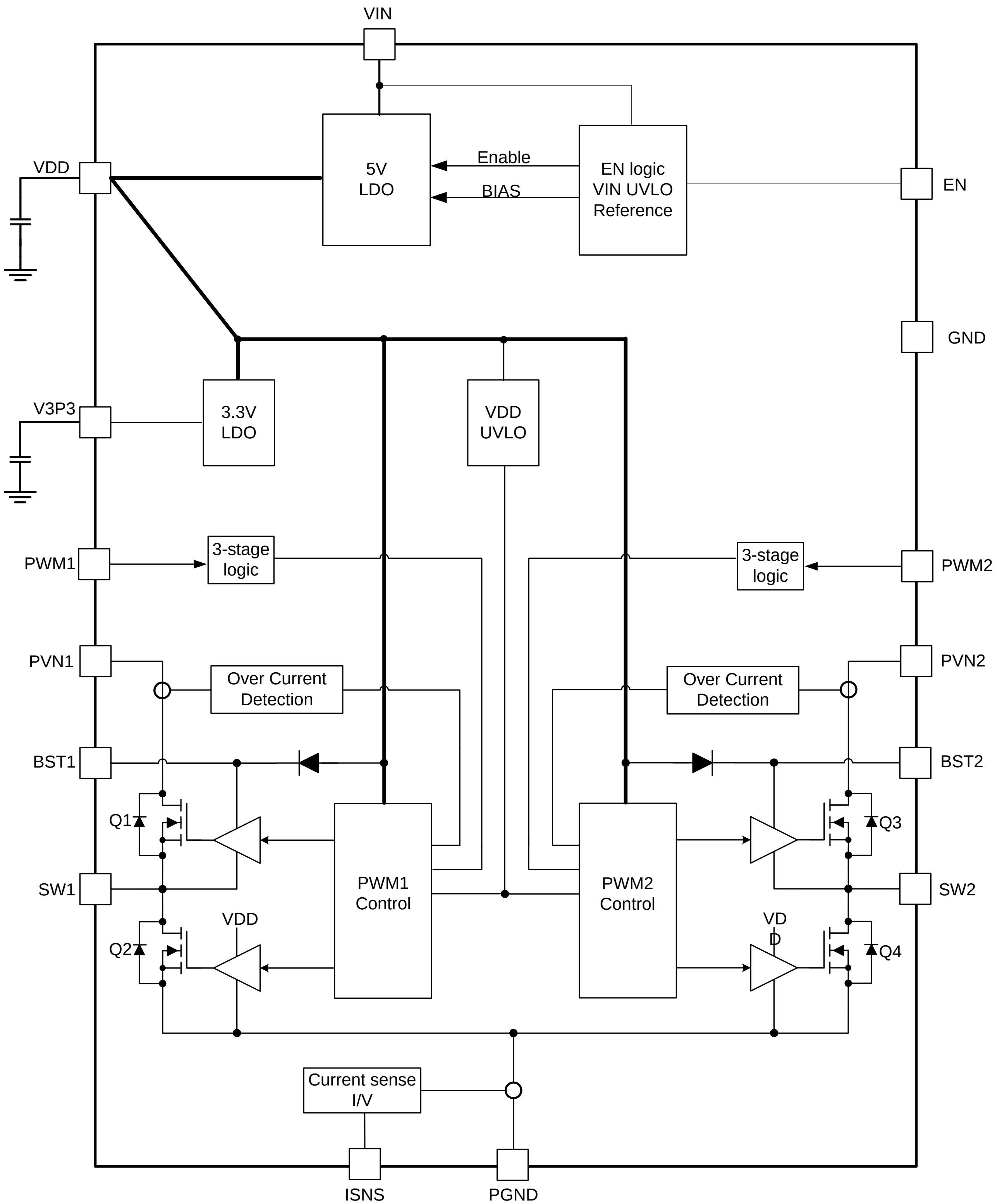


Figure 8. Functional Block Diagram

Overview

The SCT63140 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63140 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 15V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63140 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63140 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the 5V output LDO enables at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after 5V LDO works, and also the V3V. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider(R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

— 1 (1)

— (2)

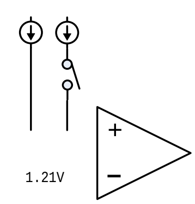


Figure 9. System UVLO by enable divider

5V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63140 integrate full bridge power stage with only 16mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63140 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63140 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1V/A. The equation 3 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

(3)

3.3V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Thermal Shutdown

The SCT63140 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

Application Waveforms

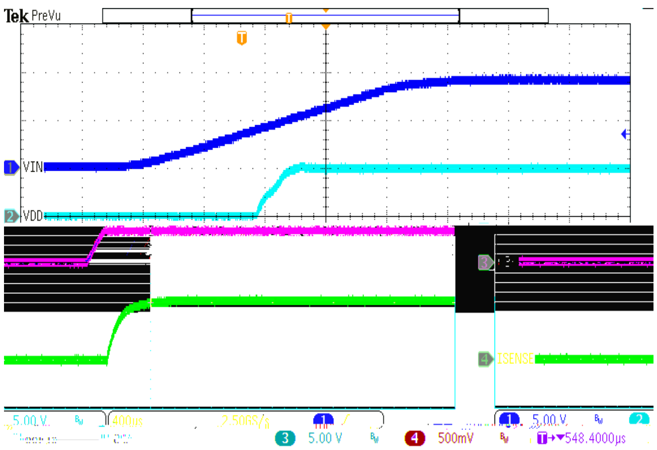


Figure 12. Power Up

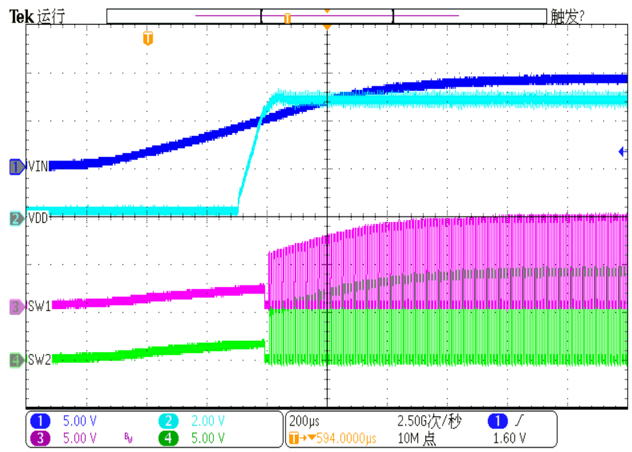


Figure 13. Power Up

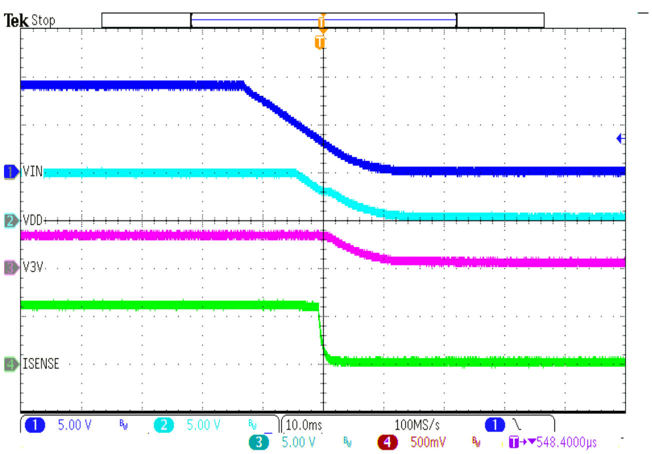


Figure 14. Power Down

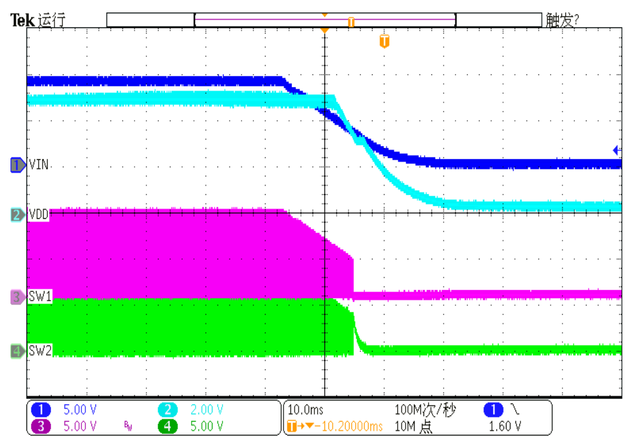


Figure 15. Power Down

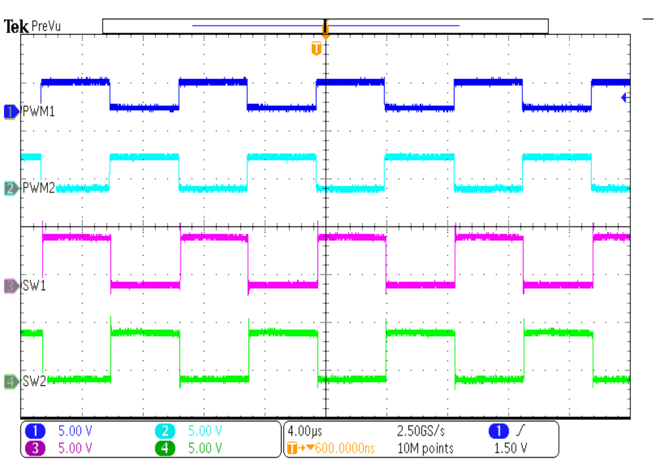


Figure 16. Full bridge @Vin=5V, RX=5W

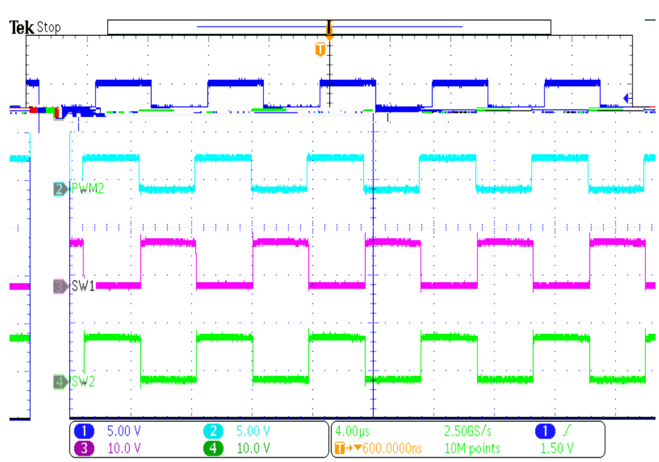
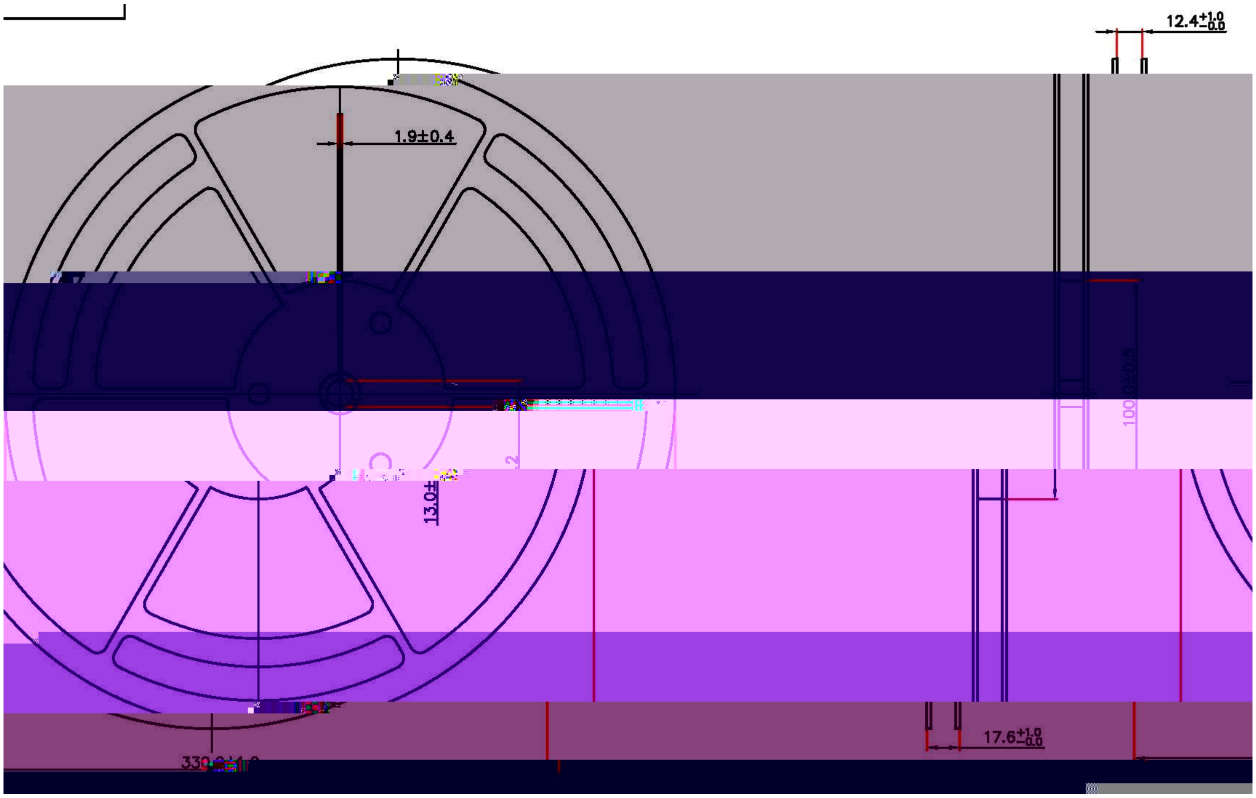


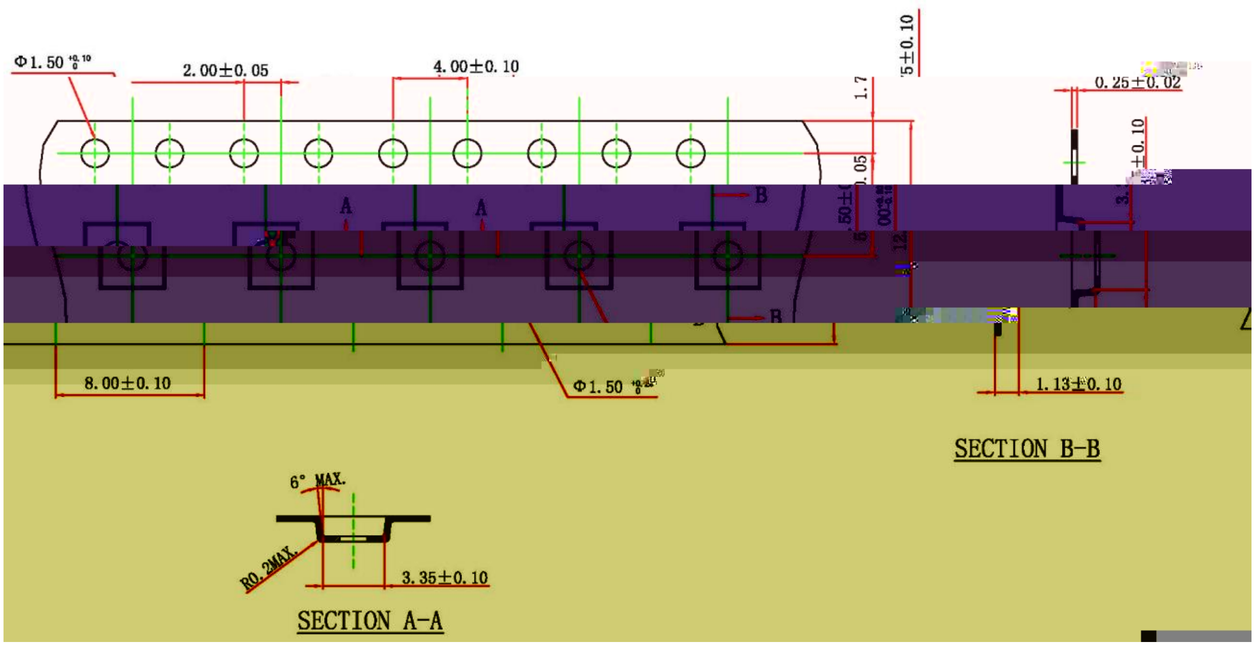
Figure 17. Full bridge @Vin=9V, RX=10W

FCQFN-15L (3x3) Package Outline Dimensions

		Symbol	Dimensions in Millimeters		
			Min.	Nom.	Max.
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2		0.55	
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.20	0.25	0.30
		b1	0.25	0.30	0.35
BODY SIZE	X	D	3.00 BSC		
	Y	E	3.00 BSC		
LEAD PITCH		e	0.50 BSC		
		e1	0.775 BSC		
		e2	0.525 BSC		
LEAD LENGTH		L	0.30	0.40	0.50
		L1	0.225	0.325	0.425
		L2	1.65	1.75	1.85

Orderable Device	Package Type	Pins	SPQ
SCT63140FMAR	QFN 3mmx3mm	15	5000





PN	DESCRIPTION	COMMENTS
SCT63240	20W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter Integrate a 5V-1A Step-down DC/DC converter compared with SC63140.	• VIN Input Voltage Range: 4.2V-20V • PVIN Input Voltage Range: 1V-17V • Up to 20W Power Transfer •

Silicon Content Technology Co., Ltd.
#1 Floor 2 Building 15, Yard 33 Dijin Road, Haidian District, Beijing 100095
TEL (8610) 64779806 FAX: (8610) 64779806 www.silicontent.com