VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	10	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
SW	11	Switching node of the boost converter.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	12	V
V_{OUT}	Output voltage range	4.5	12.6	V
[redacted]	Operating junction temperature	-40	150	°C

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		12	V
V_{OUT}	Output voltage range		4.5		12.6	V
V_{IN_UVLO}	Input UVLO					

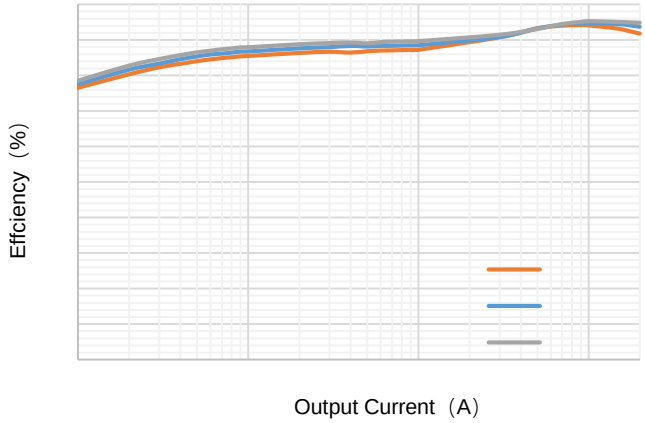

Figure 1. SCT1270 Efficiency vs Load Current, Vout=9V

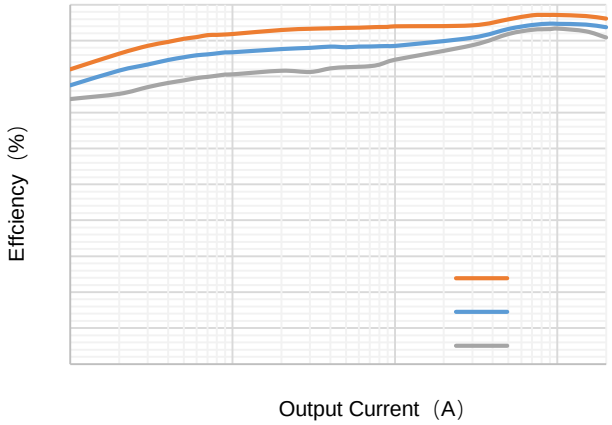

Figure 2. SCT1270 Efficiency vs Load Current, Vin=3.6V

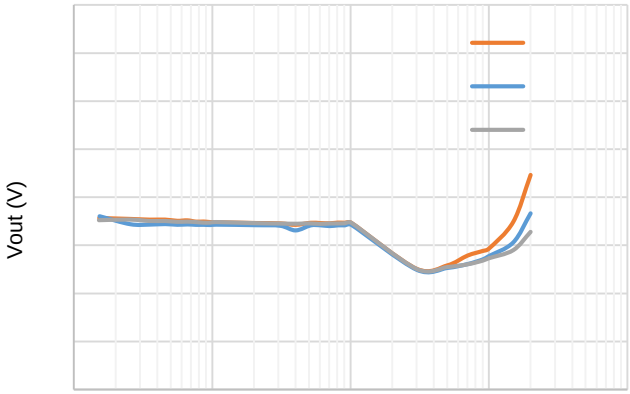

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

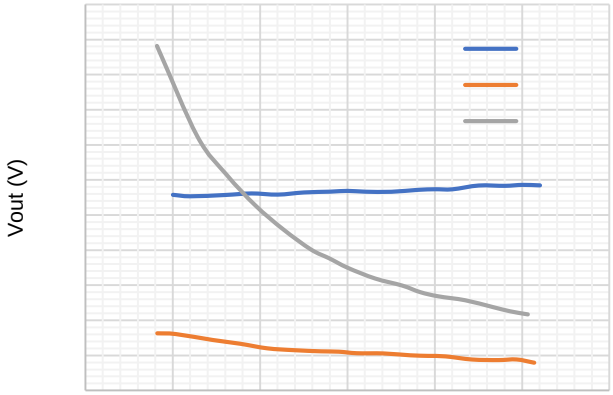

Figure 4. Line Regulation, Vout=9V

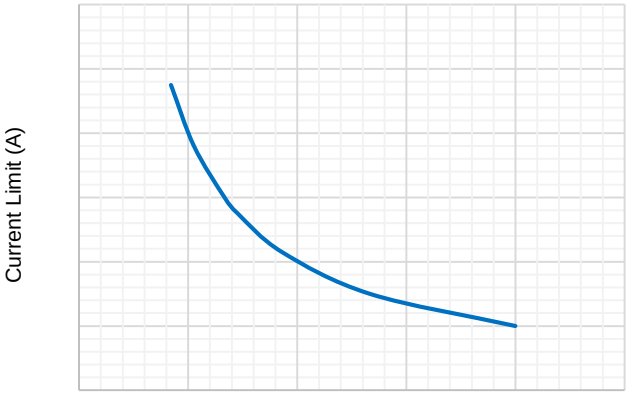

Figure 5. Current Limit VS Setting Resistance

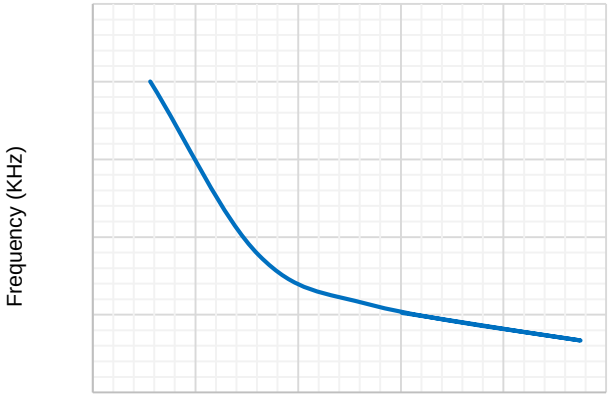

Figure 6. Switching Frequency VS Setting Resistance

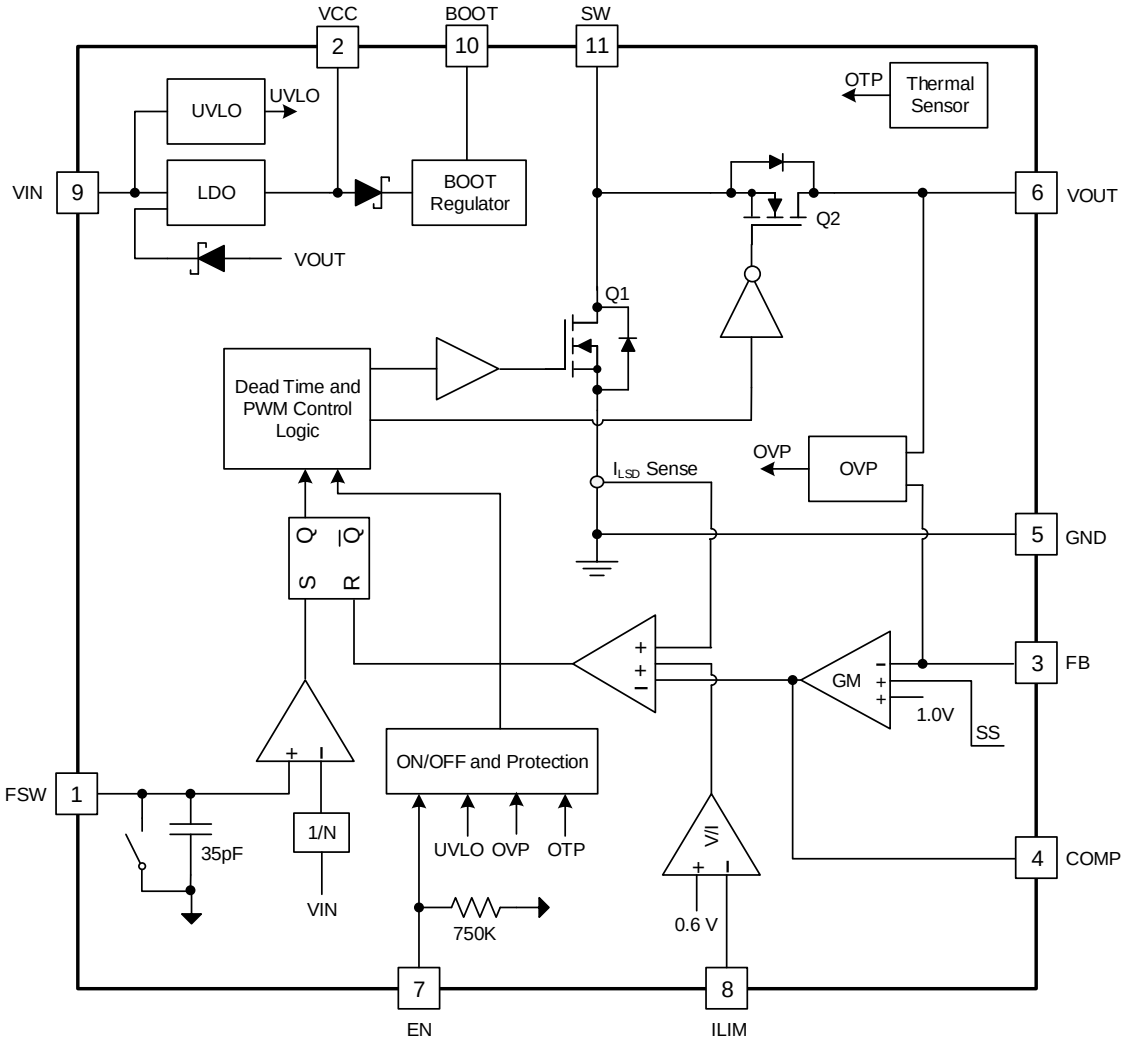

Figure 7. Functional Block Diagram

(minimum 0.4V). An internal 75 the ground. Floating EN pin automatically disables the device.

The SCT1270 features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1270 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on

and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SCT1270 delivers, the output voltage increases above the nominal setting output voltage. The SCT1270 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the SCT1270 keeps the efficiency above 70% even when the load current decreases to 1 mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 17.

Thermal Shutdown

Once the junction temperature in the SCT1270 exceeds 164 C, the thermal sensing circuit stops switching until the junction temperature falling below 140 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

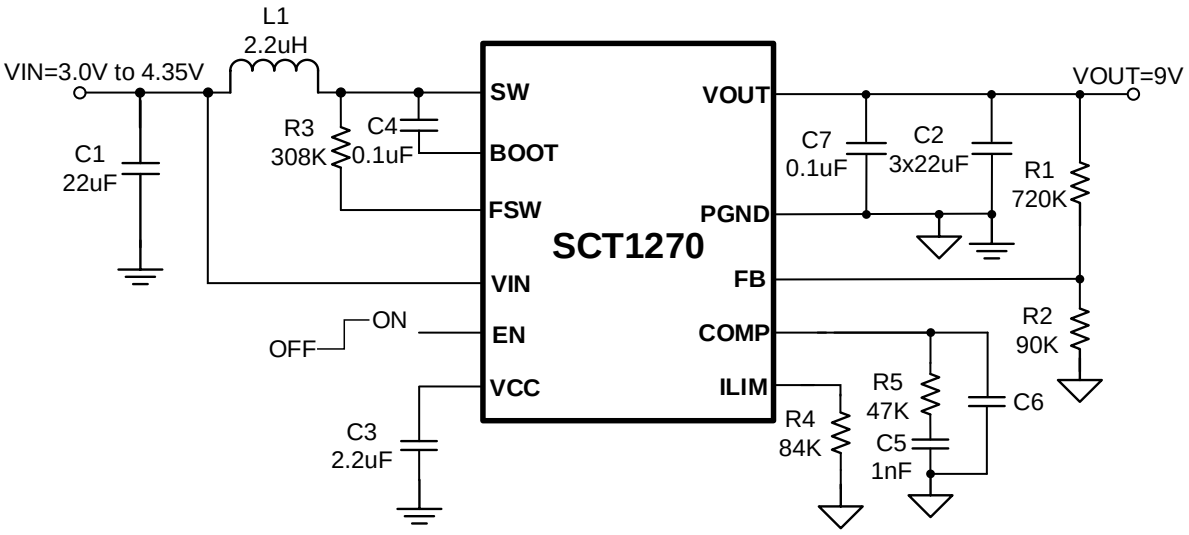

Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.35V
Output Voltage	9V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	500 kHz
Operation Mode	PFM

Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for

Inductor Selection

The performance of ansient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boost converter, calculate the inductor DC current as in equation 6

$$= \frac{\times}{\times} \quad (6)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
-

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 7

$$= \frac{1}{\times \left(\frac{1}{-} + \frac{1}{}\right) \times} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 8.

$$= \quad + \frac{}{2} \quad (8)$$

Set the current limit of the SCT1270 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed

Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT1270. Verify whether the recommended inductor can support the user's target application with the previous

calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used on SCT1270 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325180					

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

$$(\ ) = \frac{\times (1 - \ )}{2 \times} \times \frac{(1 + \frac{}{2 \times})(1 + \frac{}{2 \times})}{1 + \frac{}{2 \times}} \quad (11)$$

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.14

$$= \frac{1}{2 \times \quad \times} \quad (12)$$

where

- C_O is the output capacitance

$$= \frac{1}{2 \times \quad \times} \quad (13)$$

where

- ESR is the equivalent series resistance of the output capacitor.

$$= \frac{\times (1 - \ )^2}{2 \times} \quad (14)$$

The COMP pin is the output of the internal trans-conductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$(\ ) = \frac{\times \quad \times}{(1 + \frac{}{2 \times \quad _1})(1 + \frac{}{2 \times \quad _2})} \times \frac{(1 + \frac{}{2 \times})}{} \quad (15)$$

where

- GEAm0 g0 GβBCC}TJETQq54 327.53 378.07 44.544 reW* nBT/6.02 44.544 reW* nBT/F3 9.96 Tf1 0 0 1 543.82 349.25 Tm0 g0 G[5)]TJETQq0e78.4

$$_6 = \frac{\times}{5} \quad (18)$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

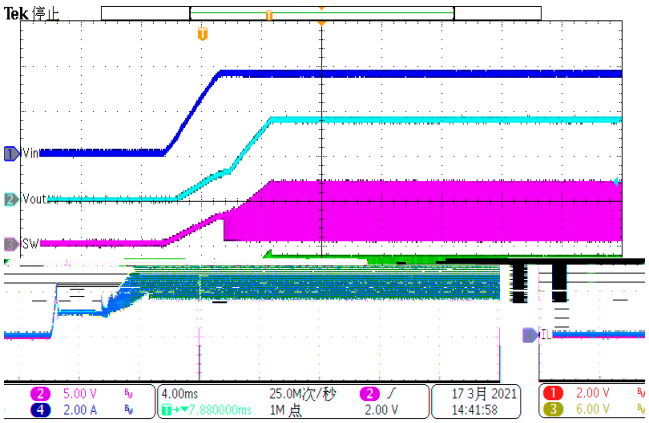

Figure 9. Power up

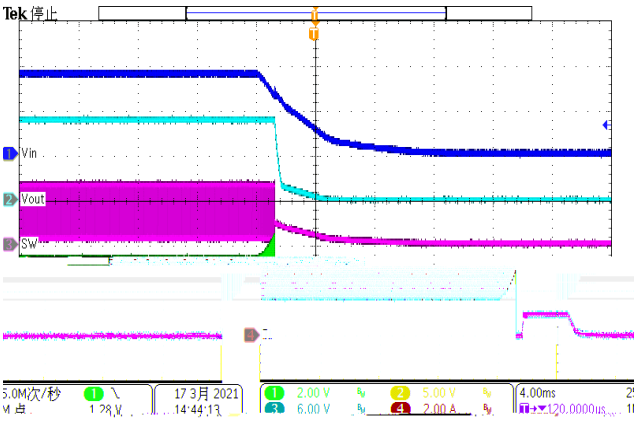

Figure 10. Power down

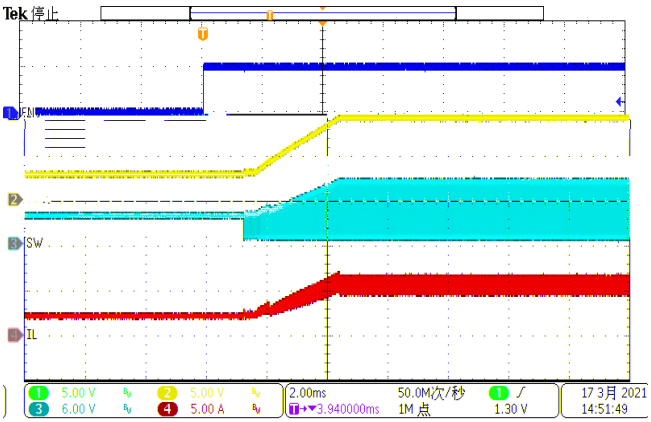

Figure 11. EN Power up (Iload=2A)

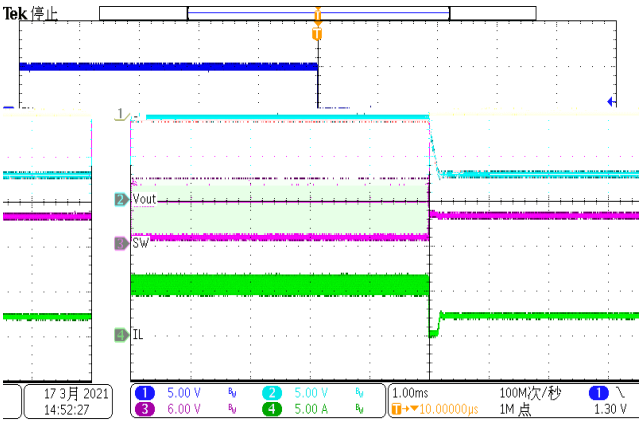

Figure 12. EN Power down(2A)

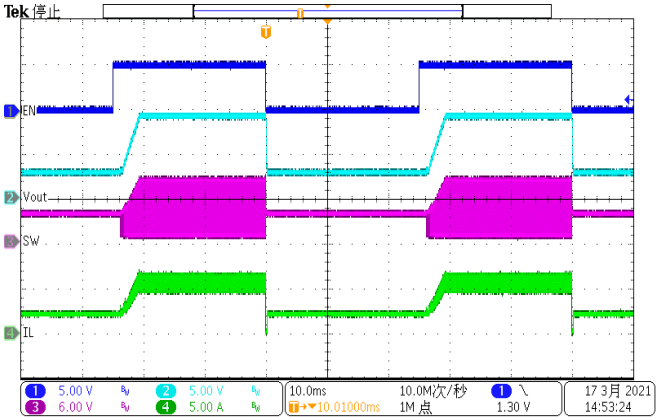

Figure 13. EN toggle (Iload=2A)

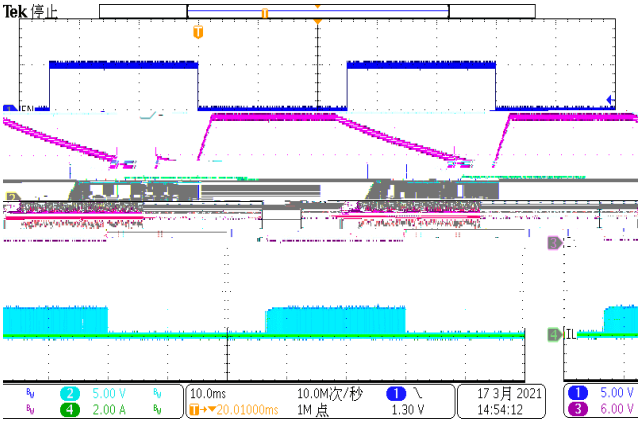

Figure 14. EN toggle (Iload=10mA)

Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

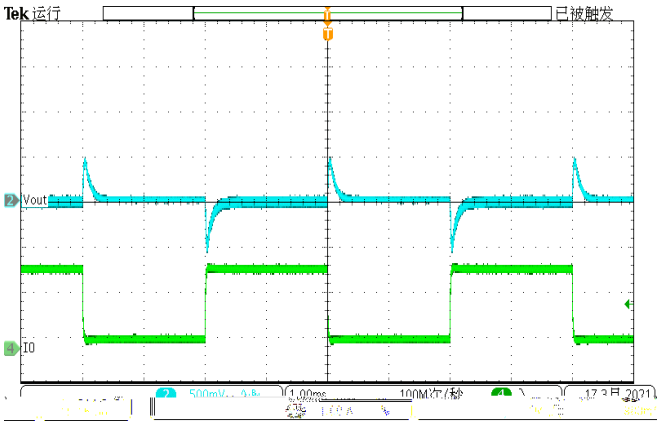

Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

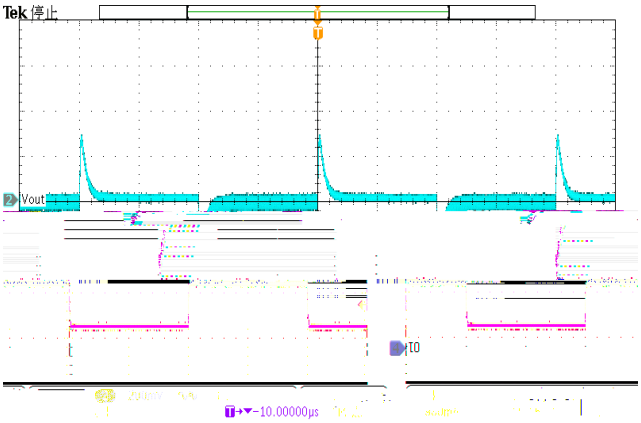

Figure 16. Load transient (0.5A-1.25A, 1.6A/us)

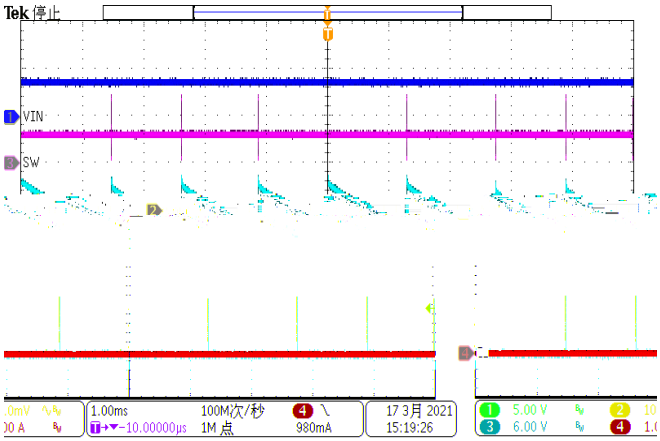

Figure 17. Steady state (Iload=0A, PFM)

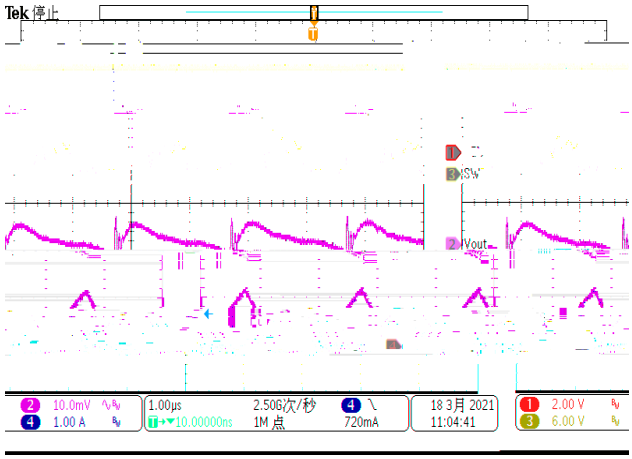

Figure 18. Steady state (Iload=150mA, PFM)

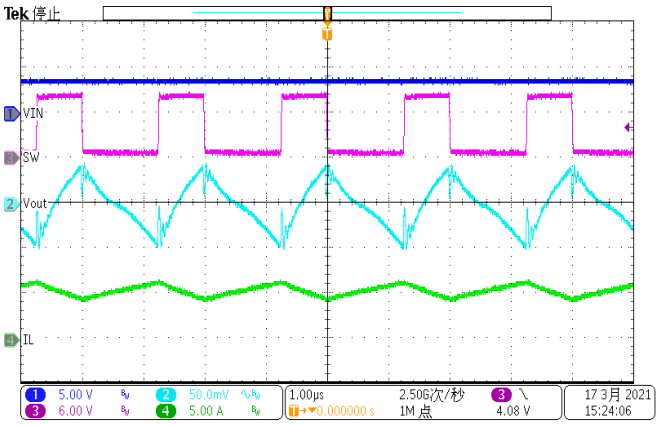

Figure 19. Steady state (Iload=2A)

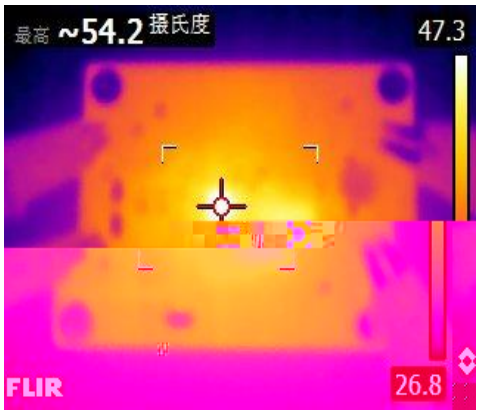

Figure 20. Thermal, Vin=3.6V, Vout=9V, Iload=2A

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for output capacitor is critical for the performance of SW ringing voltage. Place the 0.1uF output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The SW, VOUT and GND pad under the chip should always be soldered well to the board for thermal, mechanical strength and reliability. Improper soldering will cause SW higher ringing and overshoot besides downgrading thermal performance.

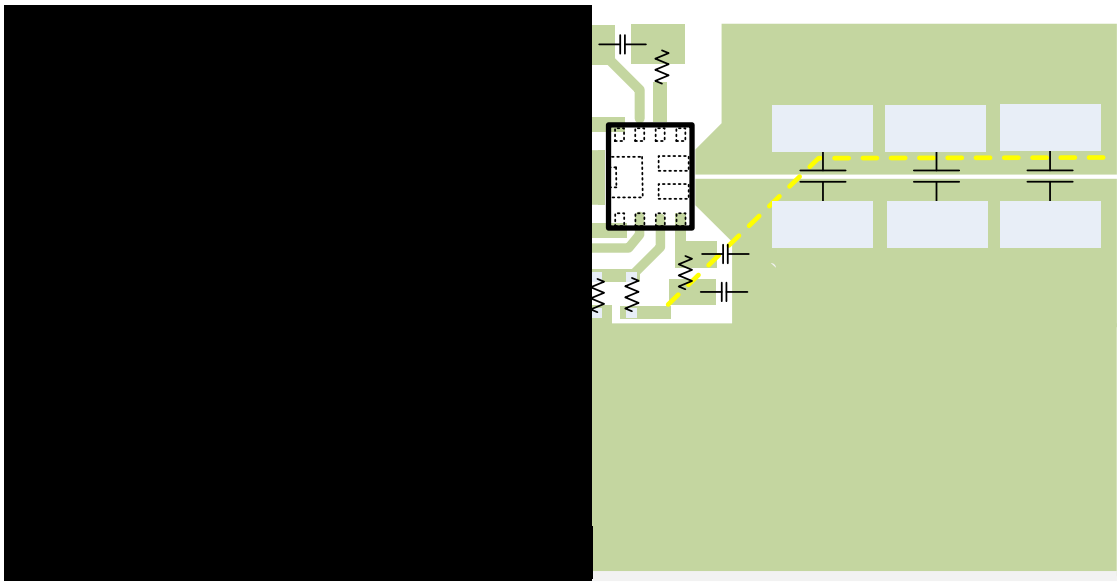

Figure 21. PCB Layout Example Top Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

$$(\quad) = \frac{150 -}{\theta JA} \tag{19}$$

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT1270 QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

Device	Package Type	Pins	SPQ
SCT1270FQAR	QFN 2.5x2x0.75	11	3000