V Vin, 2A Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Voltage: 4.2-17V
- 2A Continuous Output Current with Integrated 90m /65m FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 135uA
- Cycle-by-Cycle Current Limiting
- Internal 2.5ms Soft-Start Limits the inrush current
- Fixed 750kHz Switching Frequency
- Input Under-Voltage Lockout
- Power save mode at light load
- Over-Temperature Protection
- Available in a SOT563 and TSOT23 Package

APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

DESCRIPTION

The SCT2220 is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 2A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

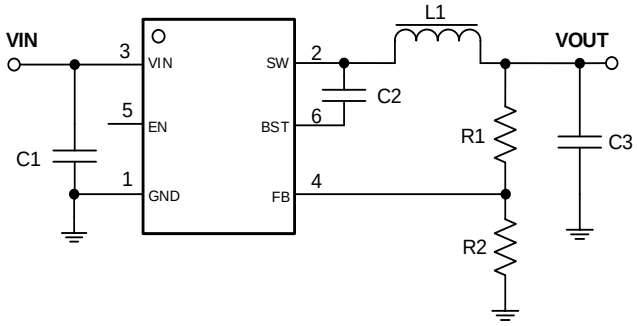
With 750kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2220 adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

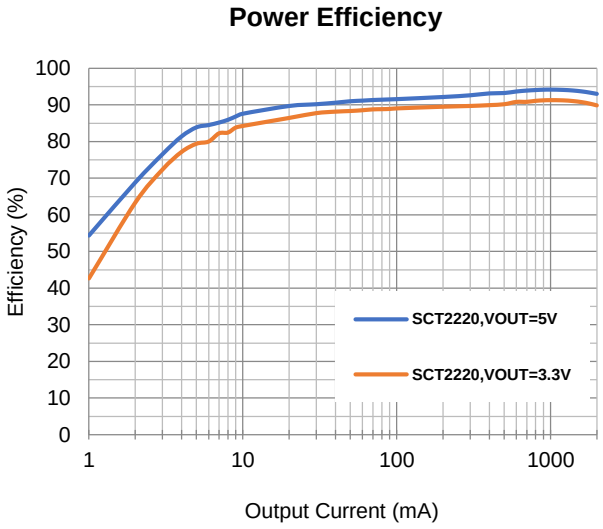
The devices operate in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2220 requires a minimal number of external components and are available in a space-saving SOT563 and TSOT23 package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev 1.0 : Released to Market

Rev 1.3: Update Iq in page1 and correct typo in EC table

DEVICE ORDER INFORMATION

PART NUMBER

PIN FUNCTIONS

NAME	PIN NUMBER		PIN FUNCTION
	SOT563	TSOT23	
VIN	1	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
SW	2	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
GND	3	1	Power ground. Must be soldered directly to ground plane.
BST	4	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
EN	5	5	Enable logic input. Floating the pin enables the device. The device has precision enable thresholds 1.2V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
FB	6	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output vo70.1T.63 E Tm20 1 314.45 477C

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.9 300	4.15	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1.5	5	uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=12V. BST-SW=5V		135		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.2	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN}	Enable pin input current	EN=1V	1	1.5	2	uA
		EN=1.5V		6.8		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			90		
R_{DSON_L}	Low side FET on-resistance			65		
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		0.78	0.8	0.82	V
Current Limit						
I_{LIM_LSD}	LSD valley current limit		2	2.8	3.6	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V		750		kHz
t_{ON_MIN}	Minimum on-time*			90		ns
t_{OFF_MIN}	Minimum off-time			220		ns
Soft Start Time						
t_{SS}	Internal soft-start time			2.5		ms
Protection						
T_{SD}	Thermal shutdown threshold* Hysteresis	T_J rising		160 20		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

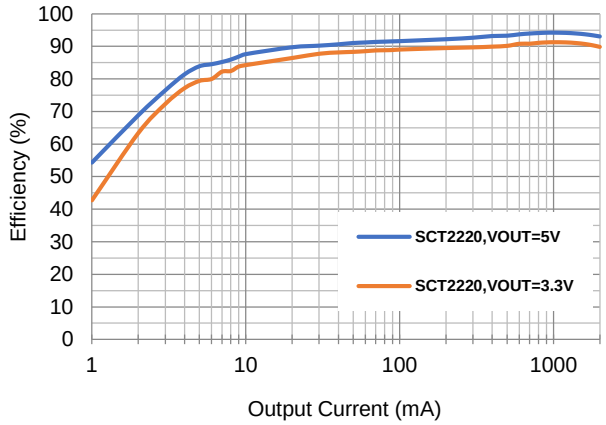


Figure 1. SCT2220 Efficiency, Vin=12V

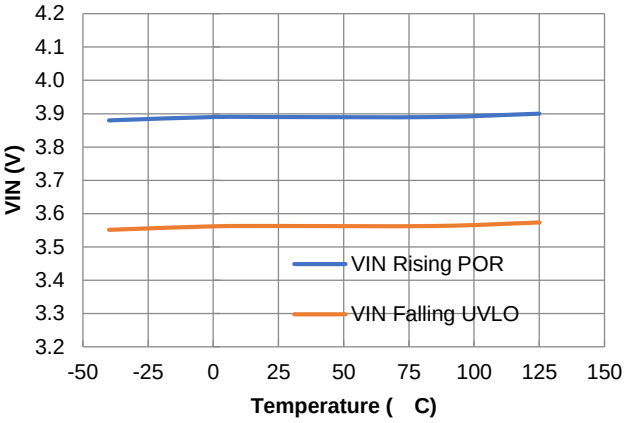


Figure 2. UVLO Vs. Temperature

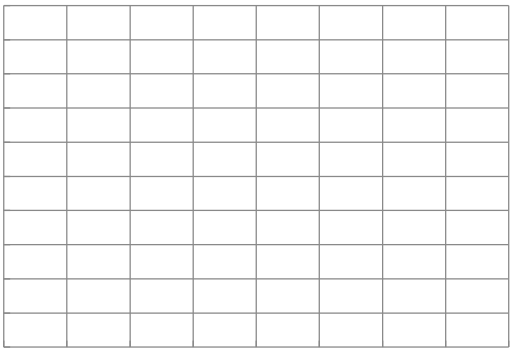


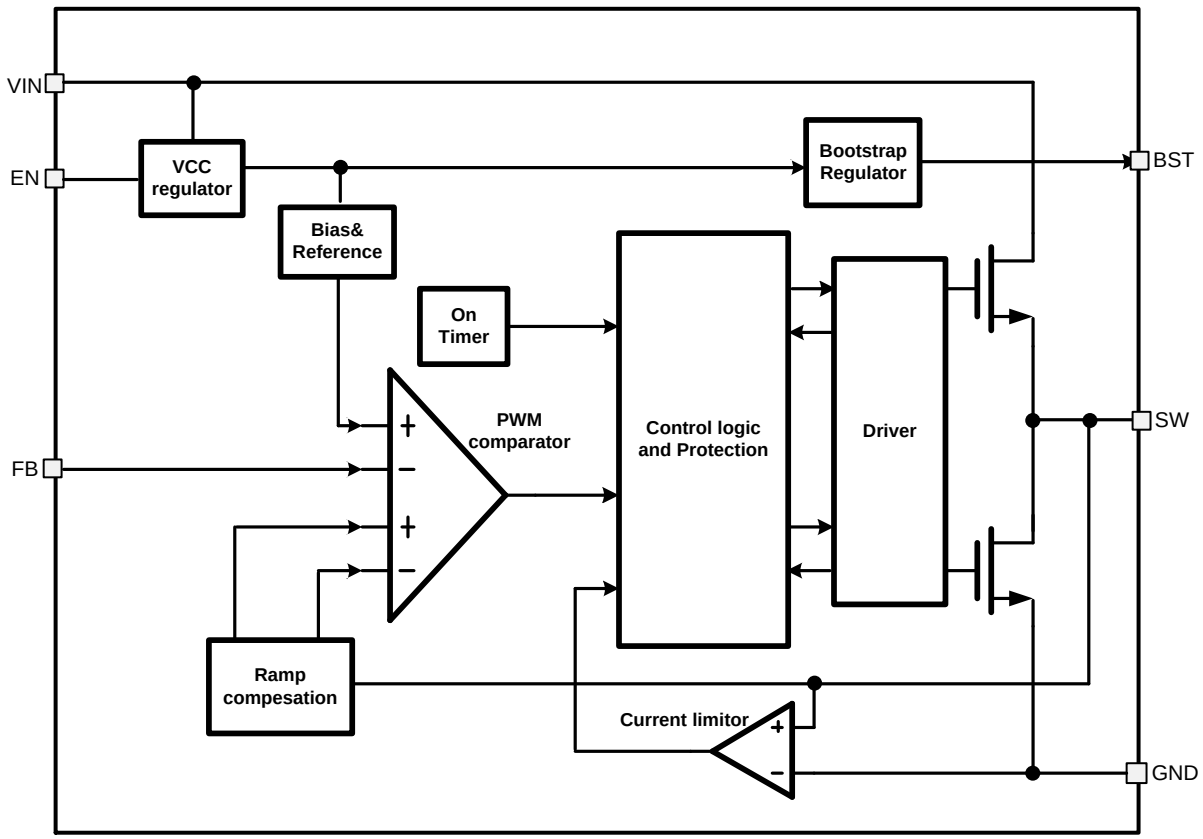
Figure 3. Line Regulation

Figure 4. Load Regulation

Figure 5. Feedback Voltage vs. Temperature

Figure 6. Quiescent Current vs. Temperature

FUNCTIONAL BLOCK DIAGRAM



Under Voltage Lockout UVLO

The SCT2220 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.9V with VIN rising and shutdown threshold is 3.6V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2220 enables all functions and the device starts soft-start phase. The SCT2220 has the built in 2.5ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 5.3uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (3) and (4).

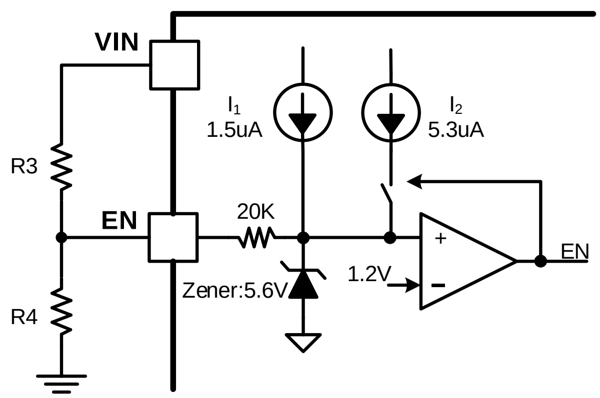


Figure 7. Adjustable VIN UVLO

(3)

(4)

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=5.3uA
V_{ENR}=1.2V
V_{EMF}=1.1V

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will dropped below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2220 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

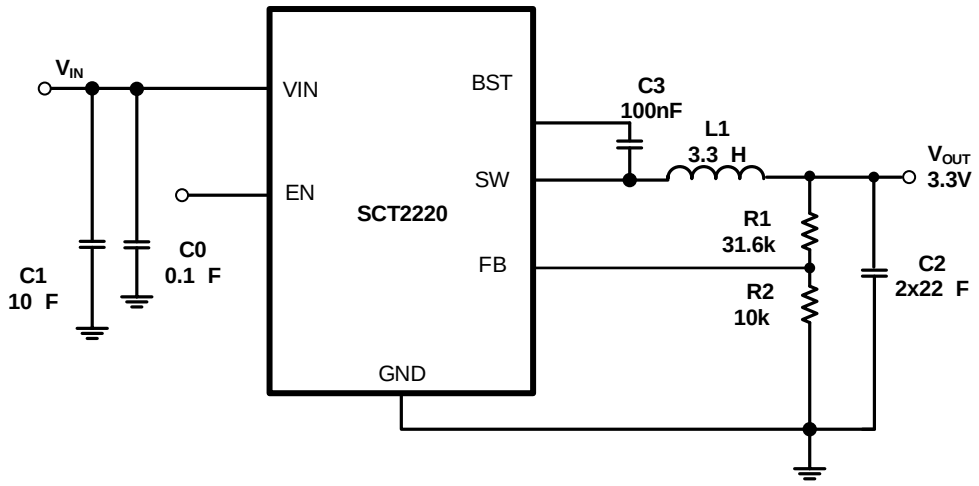


Figure 8. 12V Input, 3.3V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	2A
Switching Frequency	750kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 for the decoupling capacitor and a 0.1 to be placed as close as possible to the VIN pin of the SCT2220.

Use Equation (5) to calculate the input voltage ripple:

(5)

Where:

C_{IN} is the input capacitor value
f_{sw} is the converter switching frequency
I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of

applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of avior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (6).

(6)

Where:

K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Output Feedback Resistor Divider Selection

The SCT2220 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (8) to calculate the resistor divider values.

(8)

(nF)

Table 2. Recommended Component Selections

Output Voltage (V)	SCT2220 L (µH)	[redacted]	C2 (µF)	C3 (nF)

Application Waveforms

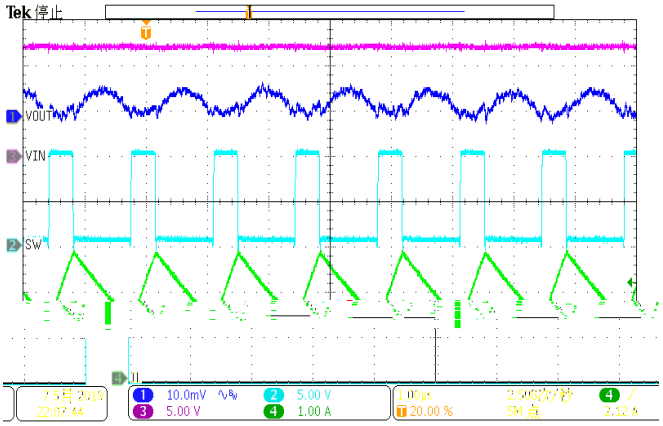


Figure 9. SW node waveform and Output Ripple
VIN=12V, IOUT=2A

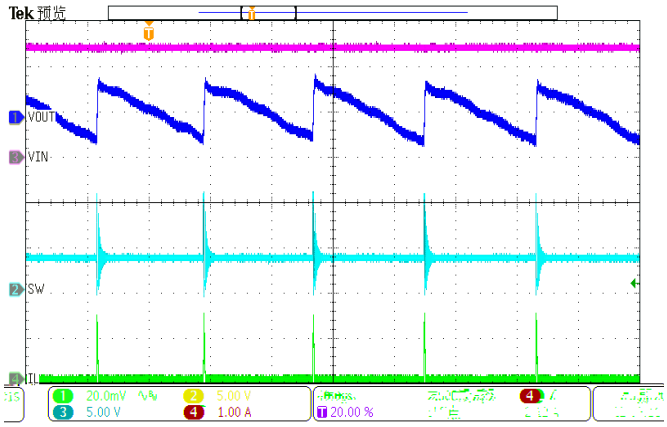


Figure 10. SW node Waveform and Output Ripple
VIN=12V, IOUT=10mA

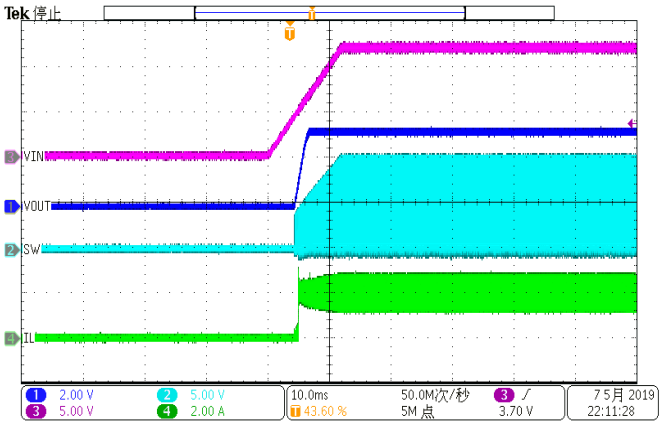


Figure 11. Power Up
VIN=12V, VOUT=3.3V, IOUT=2A

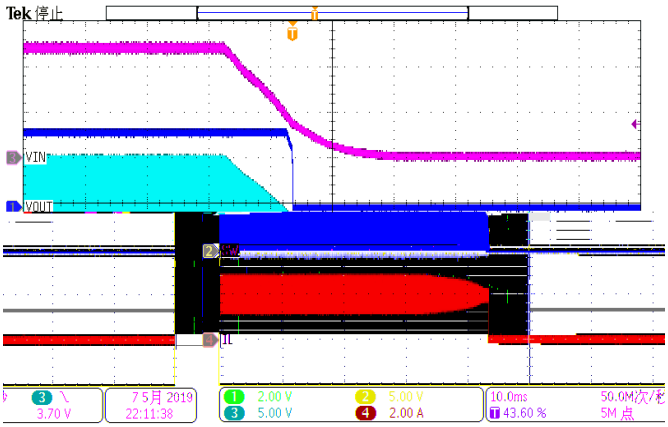


Figure 12. Power Down
VIN=12V, VOUT=3.3V, IOUT=2A

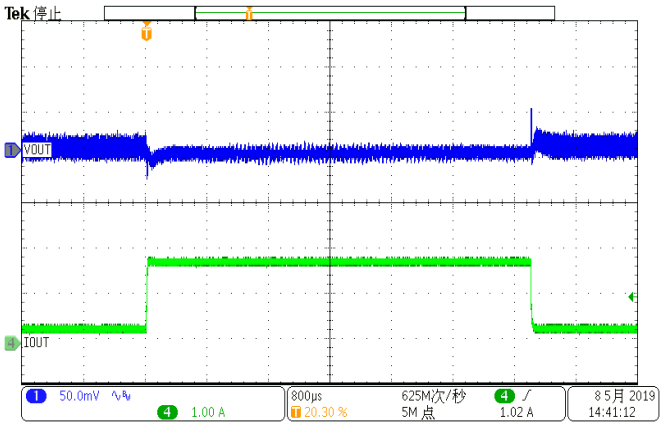


Figure 13. Load Transient
VOUT=3.3V, IOUT=0.2A to 1.8A, SR=250mA/us

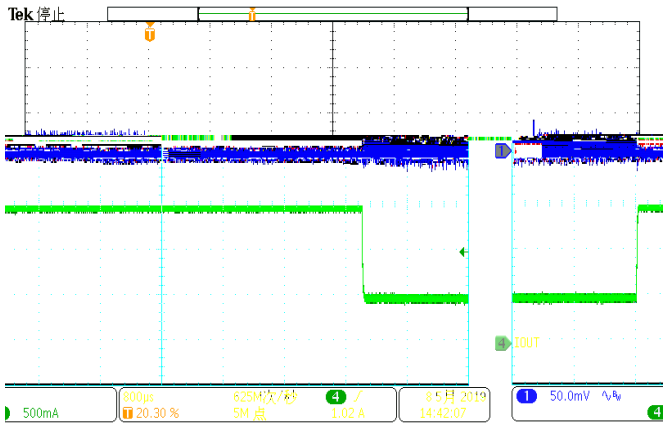


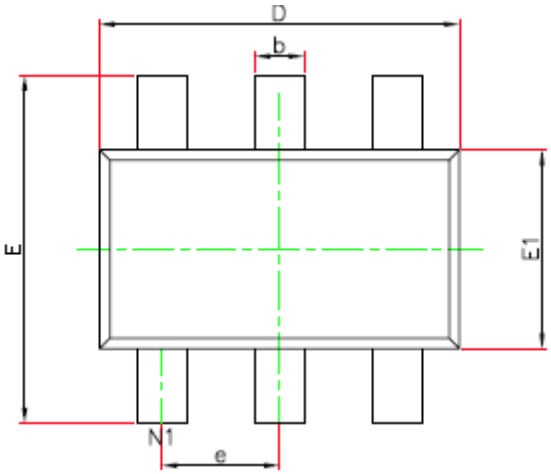
Figure 14. Load Transient
VOUT=3.3V, IOUT=0.5A to 1.5A, SR=250mA/us

Layout Guideline

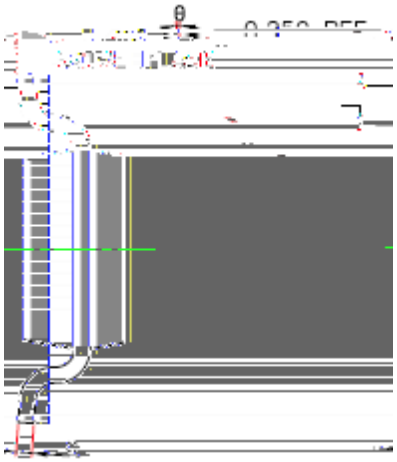
The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15 is the recommended PCB layout of SCT2220.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias

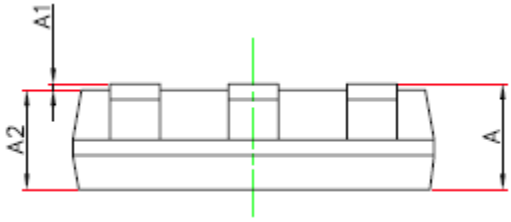
PACKAGE INFORMATION (TSOT23-6)



TSOT23-6 TOP VIEW



TSOT23-6 BOTTOM VIEW



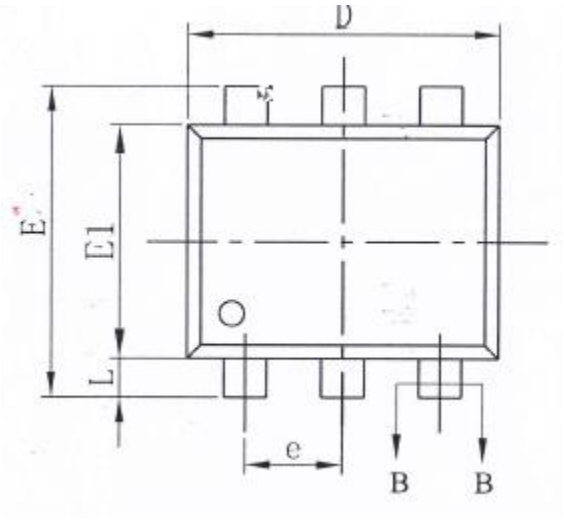
TSOT23-6 SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-------		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
	0		8

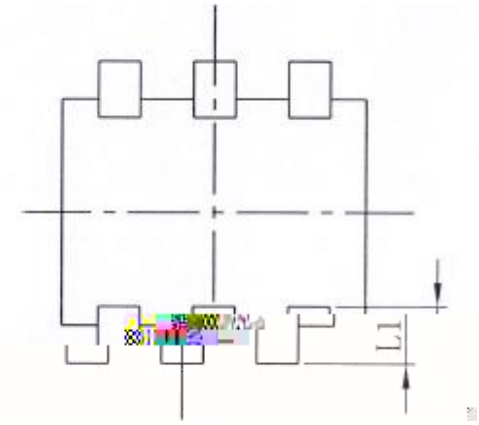
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

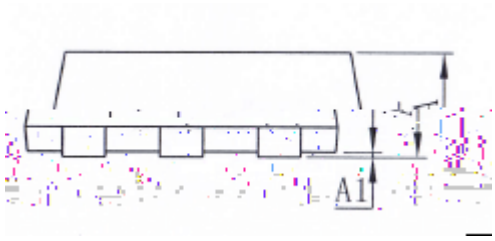
PACKAGE INFORMATION (SOT563)



SOT563 TOP VIEW



SOT563 BOTTOM VIEW



SOT563 SIDE VIEW

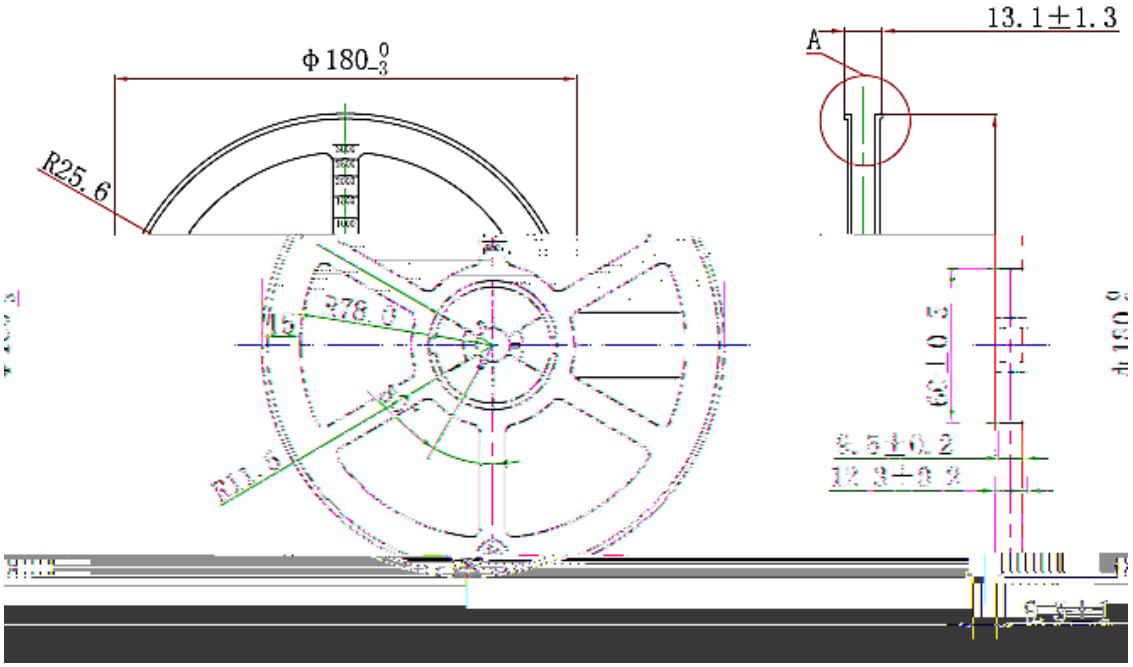
SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.53		0.6
A1	0.000		0.05
b	0.19		0.27
b1	0.18	0.2	0.23
c	0.11		0.16
c1	0.1	0.11	0.12
D	1.5	1.6	1.7
E	1.5	1.6	1.7
E1	1.1	1.2	1.3
e	0.50BSC		
L	0.1	0.2	0.3
L1	0.2	0.5	0.4

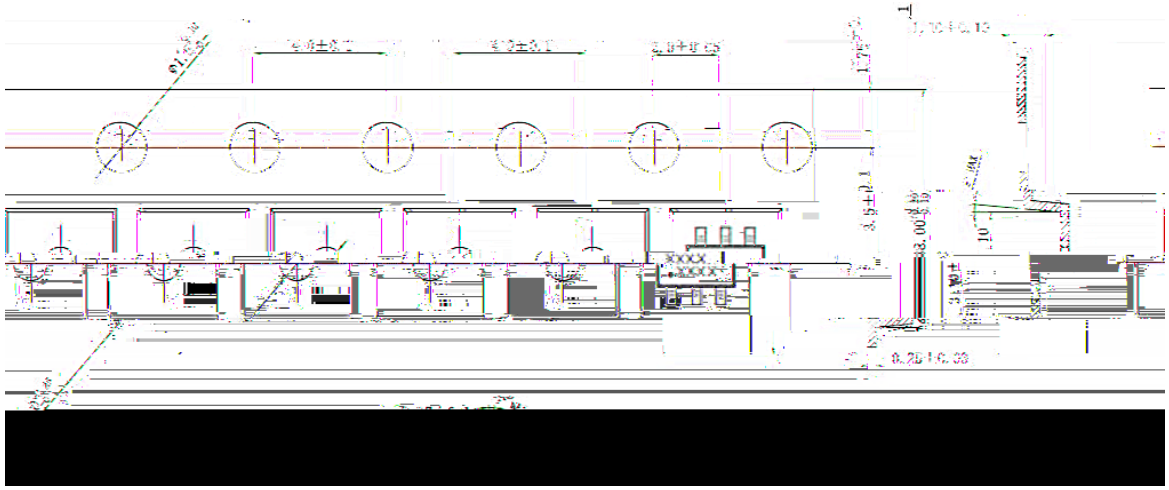
NOTE:

7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
12. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT2220TVBR	TSOT23-6L	6	3000





Feeding Direction

